FuturePlus Systems Corporation

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FS4400 PCI Express State Analysis Probe User Manual

For use with Agilent Logic Analyzers

Revision – 2.0

How to reach us

For Technical Support:
FuturePlus Systems Corporation
36 Olde English Road
Bedford NH 03110
TEL: 603-471-2734
FAX: 603-471-2738
On the web http://www.futureplus.com

For Sales and Marketing Support:
FuturePlus Systems Corporation
TEL: 719-278-3540
FAX: 719-278-9586
On the web http://www.futureplus.com

FuturePlus Systems has technical sales representatives in several major countries. For an up to date listing please see http://www.futureplus.com/contact.html.

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Introduction

How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the PCI Express Bus** chapter introduces you to the FS4400 and lists the minimum equipment required and accessories supplied for PCI Express bus analysis.
- The **State Analysis** chapter explains how to configure the FS4400 to perform state analysis on your PCI Express bus.
- The **Transaction Viewer** chapter is a brief overview of this application software that integrates with the FS4400 Protocol Decoder. For more detail on its operation refer to the FS1150 User manual on the FuturePlus Systems documentation CD.
- The **General Information** chapter provides information on the operating characteristics, and cable header pinout for the FS4400 probe.

Definitions

The following terms are used to describe aspects of the PCI Express bus:

- Channel - One differential signal (2 wires).
- PCIe Lane - A pair of differential signals running in opposite directions (4 wires).
- PCIe Link - A bidirectional interface made with two sets of unidirectional signals. A Link consists of 1, 2, 4, or 8 lanes.
- Link - One direction of a PCIe link. The FS4400 handles 1 or 2 links at a time, independently. This supports probing of both directions of a PCIe link, or probing of a pair of unrelated one-direction links. Links may be merged when displayed on the logic analyzer.
- Lane - One direction of a PCIe lane.

Analyzing the PCI Express Bus

This chapter introduces you to the FS4400 probe and lists the minimum equipment required for PCI Express Bus analysis.

The FS4400 is a High Speed, Flexible Serial bus State Analysis probe. The probe is designed to handle two directions of a link, or a single direction from each of two unrelated links, using two link-processors (A and B), at lane widths of 1, 2, 4 or 8. The probe can connect to the PCI Express target by a number of different means, including full and half-size midbus probes, x4 slot, x1 slot, x8 slot and ExpressCard interposers, or flying leads. The probe itself is controlled by the Probe Manager software, which runs under Windows and communicates with the probe via a USB cable.

The FS4400 probe “snoops” a PCI Express link without significantly degrading its signal integrity. The high speed serial signal is deserialized and processed for packet identification by the probe before being sent to the logic analyzer connections. Additionally, the probe provides trigger, filtering, and packet recognition functions. The Protocol Decoder software running on the logic analyzer provides information regarding the transactions within the captured traffic, and the Transaction Viewer provides a system level view of these transactions.

Accessories Supplied

The FS4400 product consists of the following accessories:

- The FS4400 probe, power supply and cable, 16700 Protocol Decoder SW on floppy disk, 16900 Protocol Decoder, Probe Manager, and Transaction Viewer applications on CD. A USB cable is provided for connecting the FS4400 probe to the Windows based machine that the Probe Manager is loaded on.
- This operating manual on CD, Quick Start sheet, and SW Entitlement certificates for the FS1131 16700 Protocol Decoder and FS1132 16900/Offline Viewer.

Minimum Equipment Required

The minimum equipment required for analysis of a PCI Express Bus consists of the following equipment:

- Agilent 16700 analysis frame with the 1671x analyzer card or better. **To take advantage of all options, the 16753 or better cards are the preferred cards. Alternately, a 16900 frame and 16753/4/5/6 or 169xx cards can be used.**
- Revision 2.7 or better of the 167xx Agilent Logic analysis frame software.
- Revision 3.57.1000 or better of the 1690x and 1680x Agilent Logic analysis software
- An FS4400 probing cable
- A PCI Express target bus. It is **STRONGLY recommended** that the user review and apply the probing guidelines described in the FuturePlus Systems application note “Logic Analyzer Probing Design Guide for the FS4400” when planning for use of the probe on any target system.

Probing System Overview

The architecture of the FS4400 PCI Express probe and the design of the PCI Express link to be probed should both be thoroughly understood before attempting to use the probe.

The following is a general outline of the steps to be taken when probing a new link. Read the following pages for more specific information.

The FS4400 probe requires the understanding and correct set-up of 4 different systems before a trace should be taken.

1. Probe Manager software. This software is identified as Probe Manager.exe and is on the CD that comes with the FS4410. Additionally, there is a folder within this CD that contains all the necessary USB drivers that your Windows system requires. When Windows searches for the USB drivers to load during the first connection of the FS4410, Windows **MUST be directed to load the drivers from this CD** in the system or the proper USB drivers will not load. In some cases it may necessary to temporarily disconnect the Windows system from the local network to insure that Windows does not automatically default to getting the drivers from the Internet. If the correct USB drivers are not loaded the user will see a Windows error ("Unable to load DLL") as soon as the "Run" button is used.

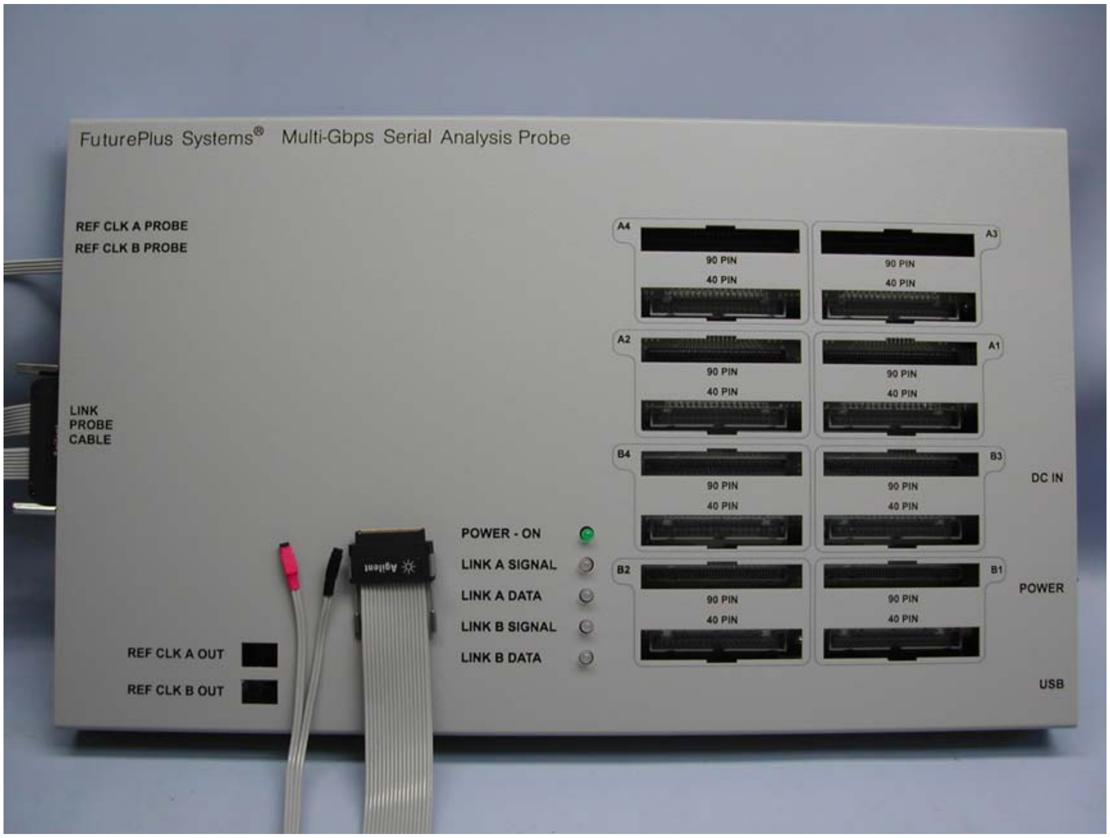
NOTE: The Microsoft .NET Framework must be on the system for the Probe Manager application to load properly.

2. FS4400 probe. This probing pre-processor requires its own DC power supply which is provided. Additionally, this probe is completely initialized, set-up and controlled by the Probe Manager software that resides on a Windows based system (PC or 168/90x frame). All communication to the FS4400 probe is by means of the USB port on the PC (or 168/90x frame). Improper or incomplete installation of either the correct USB driver or the Probe Manager software will prevent operation of the FS4400.
3. Agilent Logic Analyzer. The configuration files and Protocol Decoder for the 1670x analyzers (FS1131) are on a diskette. The files for the 168/90x analyzers (FS1132) are on a CD. Install these files as required and follow the instructions for logic analyzer module (card) interconnections and logic analyzer Pod connections to the FS4400 probe.
4. PCI-Express target platform. There are a number of different probing options, including mid-bus probe, interposer, flying lead, etc. There are also a wide variety of PCI-E link implementations besides widths of x1, x2, x4, x8, etc. There are protocol attributes such as lane inversion, data scrambling, lane reversal, and spread spectrum that need to be defined in the Probe Manager in order for the probe to capture data properly.

It is strongly recommended that the user methodically proceed in the following manner when setting up the probe. There is more detail on each step in this manual.

1. Load the Probe Manager software, configuration files and Protocol Decoder on the PC and/or 168/90x logic analyzer. Leave the CD in the system for access to the USB drivers.
2. Configure (meld) the logic analyzer cards as required, remove any adapter cables on the Pod connections and run the Agilent Logic analyzer's internal diagnostics on the cards. If the analyzer passes then make the appropriate Pod connections to the FS4400 probe.
3. Connect the appropriate probing cable(s) to the target system, power up the probe. This may result in a Windows dialog searching for the "*FTDI FTD2XX*" USB drivers; direct it to the Probe Manager CD. Check the Windows Device Manager to make sure that it loaded properly.
4. Open up the Probe Manager application and select the appropriate settings for the probe cable being used and the PCI-Express link. Check that the expected Pad assignments for the probed link show green. For the first capture turn off all the filters.
5. If the FS4400 probe LEDs are all Green and the first trace file captured on the logic analyzer has no error messages then it is a good indication that all initial settings are correct.
6. A link showing Signal LED green and Data LED orange constantly, needs settings for link width, lane reverse or lane inversion adjusted in the Probe Config window.
7. A link showing Signal LED orange or red may have a problem with the reference clock connection, or need settings for Internal/External reference clock adjusted in the Probe Config window. More information on link signal status can be seen in the Log File window.

Front Panel



The connections and features of the FS4400 probe include:

- DC input for provided external AC to DC power supply (please note that the use of any other power supply voids the warranty on the FS4400), On/Off switch and USB connections to the Windows PC/16900 where the Probe Manager software will be loaded.
- Link Probe cable connection for any 1 of the different probing cables and Reference Clock probe cable connections.
- Logic Analyzer probe connections. One set for 90 pin pod connections and a duplicate set for 40 pin pod connections. A1 – A4 are connections for 1 Link Processor, and B1 – B4 are for the other Link Processor.
- Reference Clock Probe Cable is permanently attached to the FS4400.
- LED indication of probe power on and Link status. For each link there is a pair of LEDs which have the following states:

Link A or B Signal LED color	Meaning	Link A or B Data LED color	Meaning
Green	Link OK	Green	Data clocking Into Analyzer
Dark	Loss of Signal	Dark	No Data clocking into Analyzer
Orange	Data Invalid (8b10b error)	Orange	Any Error: 8b10b, Align, Framing, Idle
Red	Receiver Fault	Red	Processor Clock Error

FS4400 Probing Cables

The FS4400 PCI Express probe can be configured with a wide variety of different probing cables dependent on what the user requires:

FS1031	Full size midbus footprint probe cable for x1, x2, x4
FS1032	½ size midbus footprint probe cable for x1, x2, x4, x8
FS1033	ExpressCard Interposer probe cable with reference clock buffer
FS1034	x1 slot Interposer probe cable
FS1035	x4 slot Interposer probe cable
FS1036	Flying lead probing cable for x1, x2, x4, x8
FS1037	x8 slot interposer cable (requires 2 FS4400 probes)
FS1038	Full size midbus footprint probe cable for x8 (requires 2 FS4400 probes)
FS1039	Full size midbus footprint probe cable for x8 (requires 2 FS4400 probes)

Cables FS1038 and FS1039 can also support x1, x2, x4 probing.

Cables FS1038 and FS1039 differ in their pinouts, the FS1039 better supports the routing of all lanes on the same surface layer.

The "PCI Express Probing Design Guide for the FS4400" provides specific information on the successful application of midbus probing and also details general requirements for the Reference Clock signal and other aspects of the link to be probed. The FS4400 manual assumes that the user is familiar with this information and has applied it.

The cable should be attached to the FS4400 and carefully secured with the 2 captive fasteners on the cable. The probing end should be attached to the target either by screwing into the retention module (midbus probe) or inserting the Interposer into the slot being probed. Use of the flying lead probe requires careful installation and mechanical support of special axial leaded "RF-resistors".

Note that use of the external Reference Clock is required when:

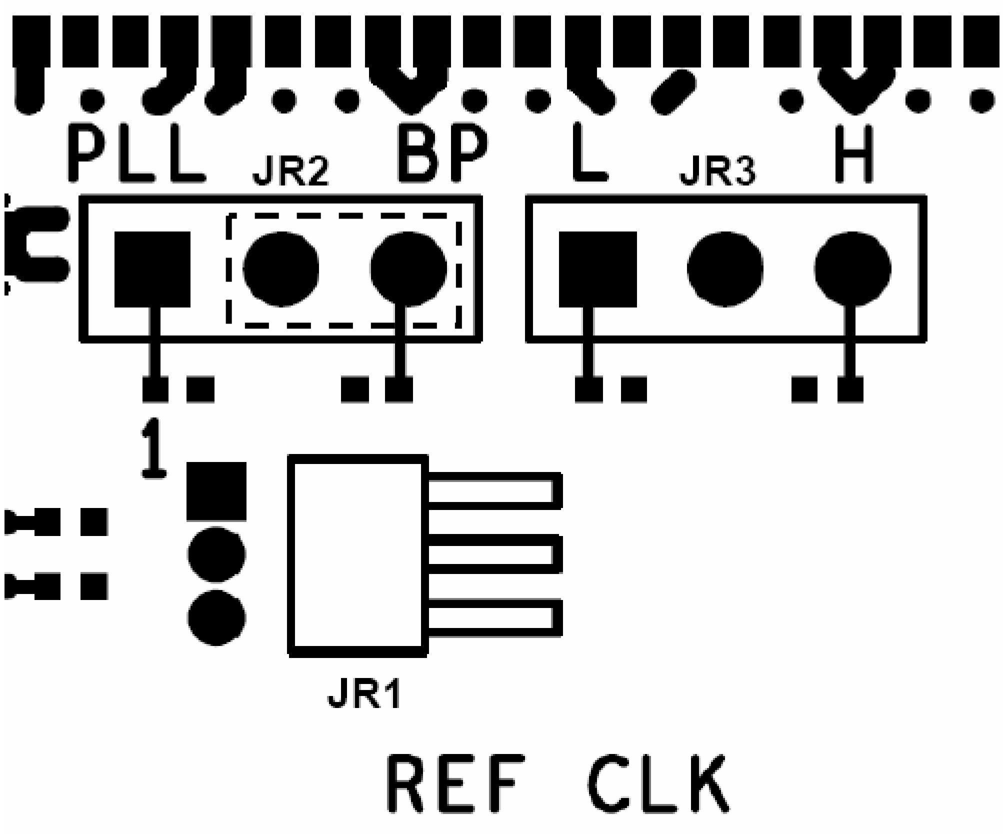
- Spread Spectrum modulated clocking is occurring.
- The target transmitter frequency is not within 100 ppm of nominal (even though the PCIe standard allows 300 ppm deviation from nominal)
- When the probe is operated in 10b mode (10-bit undecoded mode).

Interposer Probing FS1034/5/7

Due to the source terminated nature of the Reference Clock used in PCIe it is difficult to acquire a quality signal at a mid-point of the Reference Clock trace, which is where the Interposer probe sees it. In order to provide a high quality signal at the Interposer probing point these probes (FS1034/5/7) incorporate a PCIe Reference Clock buffer chip which serves to terminate this signal and then re-transmit it to both the target board and to a 3 pin connector (JR1) on the Interposer that can be used to connect the Ref. Clk cable from the FS4400 probe.

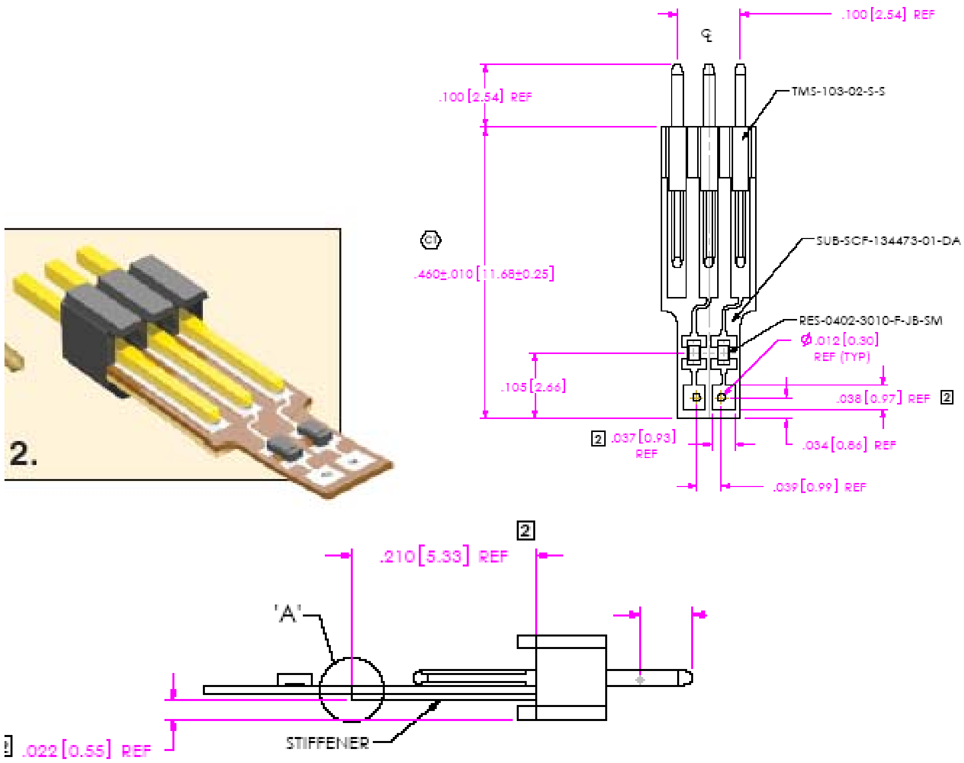
The Reference Clock Buffer chip can be operated in two modes: By-Pass or PLL. FuturePlus recommends that the Interposer probe be used in By-Pass (BP) mode. If used as a PLL it could create dynamic tracking error between the PLL used on the system board and the PLL function on the interposer during SSC operation. It is possible to use the PLL function to reduce jitter in the Reference Clock. This would require moving the JR2 jumper from connecting the center and right hand pins to connection the left hand and center pins. Additional control of the PLL mode can be provided by changing the bandwidth of the PLL from Low to High by moving the jumper at JR3. This BW function is only active when the device is in PLL mode.

The proper recommended shunt location is shown by a dashed line below:



Flying Lead Probing (FS1036 cable assembly)

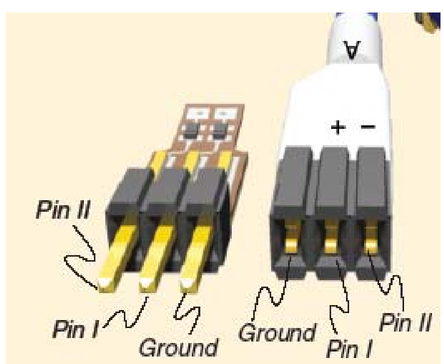
The FS1036 flying lead cable assembly allows the FS4400 probe to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb.



A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036 cable that provides detail on how to solder the flex pcb to your board. Refer to this document.

2. Polarity matters. Makes sure you know how the + and – sides of the signal are connected. Adjustment to polarity can be made in the Probe manager.



The FS1036 flying lead cable has 8 pairs of channel connectors which are labeled A-G for up to 4 channels of a link and B-H which can be used for another link. When plugging in the flex tips make sure it is a good fit into the cable connector.

Make the appropriate cable and channel selections in the Probe manager before taking any probe measurements.

ExpressCard Probing (FS1033 Interposer assembly)

The FS1033 is a cable assembly that includes a slot interposer for an ExpressCard/34 slot. The interposer is made to be of sufficient length to use without having to remove the covers on a target platform. As specified by the PCMCIA organization the ExpressCard link works as either an x1 PCI Express module or as a USB2.0 module.

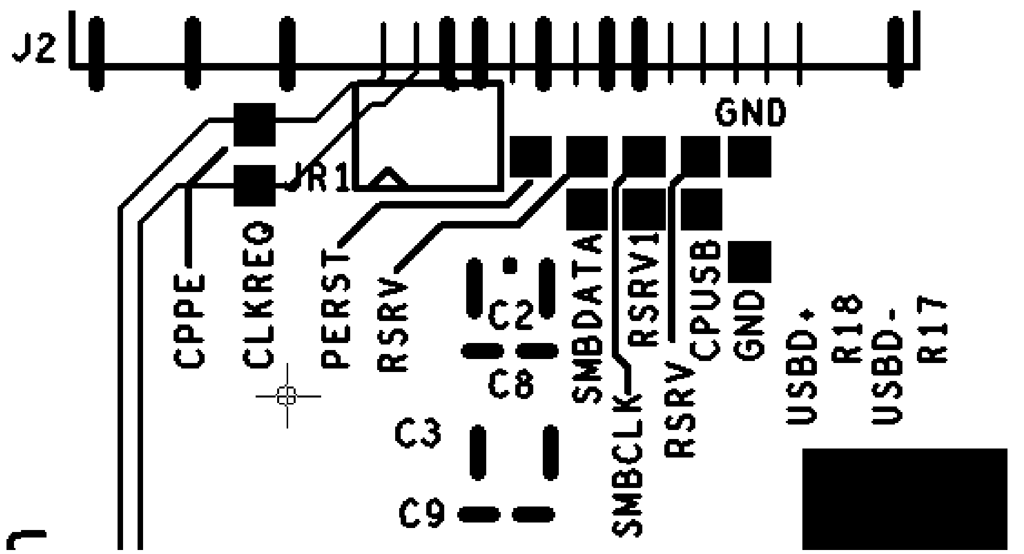
The FS1033 is a passive interposer of all signals except for the REF CLK, which is re-buffered appropriately and sent to both the ExpressCard module connector and to a Reference Clock header for use with the FS4400 probe.

To provide additional functionality, probing pads are provided on the slot interposer for all the ExpressCard signals besides PET/Rp/n (both directions of the x1 lane width links). These points are clearly labeled in the silkscreen as shown below.

Probing USB with the FS1033

This can be done by using the FuturePlus Systems FS4120 USB2.0 probe and using custom pigtail cables soldered to the pads at R17 and R18. Please contact FuturePlus Systems for these cables.

In many cases the ExpressCard module is not “hot-pluggable”, the FS1033 will have to be interposed between the target and the module before powering up the system. The REFCLK signal is provided at JR1 for use with the FS4400 probe’s cable. The x1 PCI Express signals are cabled to a standard FS4400 probe connector. Make sure all these connections are made before powering on the system or the probe.



Installing your Software for the First Time

The following outlines the software installation procedure when using the probe for the first time. Please do not attach the probe to the analyzer or computer that will be controlling the probe until told to do so.

1. Place the software CD that came with the product into the logic analyzer or computer that you will be installing the software on. In the case of a 1680x machine that does not have a CD drive, the 1680x will either have to be put on a network and the files loaded remotely or the CD files can be transferred to the 1680x from a USB drive.
2. Navigate to the installation CD using Windows explorer and click on the following files. Follow the instructions on the screen to install.*
   - FS1132.exe
   - FS1150.exe
   - FS44xx Probe Manager.exe
3. Once all the above files have been installed, connect the FS4400 to the analyzer/computer via the USB port. Power on the FS4400 probe.
4. The found new hardware wizard should appear the first time the probe is attached and powered up. Select “no, not this time” when it asks if the computer can go to Windows update to search for the software. Then select next.
5. On the next screen select the advanced option (not the recommended) to select from a specific list or location. Select next.
6. Select the CD-ROM drive to load the driver from; you do not have to select a specific directory. Select next.
7. There may be a warning that comes up about Windows XP compatibility, ignore this warning and continue with installation.
8. Click finish to complete the installation.

Once all the previous steps have completed all necessary software as well as USB drivers will be installed. This procedure only needs to be done on initial install. You may now go to the desktop and click on the Probe manager icon to start the probe manager.

*If you are installing on a PC to only control the FS4400 probe then you can omit the installation of the FS1132.exe and FS1150.exe, but you must follow the rest of the steps.

For instructions on loading configuration files please refer to the section on loading configuration files later in this manual.

Connecting the Agilent logic analyzer to the FS4400

The FS4400 is designed to enable the user to connect the FS4400 to the widest possible range of Agilent logic analyzer modules (cards). This table describes the possible configurations:

Module PN	Pods per module	Conn Style	State speed norm/turbo	16900 or 16700 Frame	Module Qty for X1 PCIe 2 “links” (state clock 125 MHz)	Module Qty for X2, X4 PCIe 2 “links” (state clock 250 MHz)	Module Qty for X8 PCIe 2 “links” (state clock 250 MHz)
16950A	4	90 pin	300/600	16900	2	2	3
16911	4	40 pin	250/500	16900	2	2	3
16910	6	40 pin	250/500	16900	2	2	2
16760	2	90 pin	200/ 800	Both	4	N/A	N/A
16753-6	4	90 pin	300	Both	2	2	3
16750-2	4	40 pin	200/400	Both	2	4	4
16717-9	4	40 pin	167/333	16700	2	4	4
16740-2	4	40 pin	200	Both	2	N/A	N/A
1680/90	-	40 pin	200	Neither	8 pods	N/A	N/A
1680x	-	40 pin	250/450	Neither	8 pods	8 pods	12 pods

For the 1690x/1680x Logic Analyzer

Use the General Purpose Probe feature in the Overview section of the 16900 Logic Analyzer application to connect the logic analyzer cables to the FS4400 probe.

For the 16700 Logic Analyzer

Connect the logic analysis cards to the FS4400.

Logic Analyzer	FS4400	Comment
Master Pod 1	A1	J clock first link
Master Pod 2	A2	
Master Pod 3	A3	
Master Pod 4	A4	
Expander Pod 1	B1	J clock second link
Expander Pod 2	B2	
Expander Pod 3	B3	
Expander Pod 4	B4	

Based on the probing needs install the appropriate modules into the Agilent logic analyzer and remove any adapter cables that may be attached to the module cables. When probing 2 directions of x1, x2, x4 links, or a single direction of an x8 link, the FS4400 drives 8 pods of signals to the logic analyzer. When probing a single direction of a x1, x2 or x4 link, the FS4400 drives 4 pods of signals to the logic analyzer.
For probing a single direction of a link, a single machine is used. For probing two directions of a link, two machines are used. A state clock is provided to each machine and the frequencies may differ slightly.

It is important before you load a configuration file you initiate a self test on all your modules installed in your logic analyzer to insure all modules are working properly.

Setting up the 167xx Analyzer

For 167XX logic analyzer installations, the FS4400 software consists of one diskette.

To install the FS4400 software, insert the diskette labeled 16700/702 Installation disk for the FS4400 into the Agilent 1670x diskette drive. From the SYSTEM ADMINISTRATION TOOLS select INSTALL under SOFTWARE. From the SOFTWARE INSTALL screen select the FLEXIBLE DISK and APPLY. Once the title appears select it and then select INSTALL.

This procedure does not need to be repeated. It only needs to be done the first time the FS4400 PCI Express State Analysis Probe is used.

When this has completed, load the appropriate configuration file from the /configs/FuturePlus/FS4400 directory. Refer to the table on the following pages for a list of analyzers and corresponding configuration files.

Setting up the 1690x or 1680x Analyzer

The 16900 Analyzer is a PC based application that requires a PC running the Windows OS with the Agilent logic analyzer software installed or a 169xx frame.

Before installing the protocol decoder for the FS4400 on a PC you **must** install the Agilent logic analyzer software first. Once the Agilent logic analyzer software is installed, you can install the FS4400 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the FS1132.exe file on the CD-ROM disk and then double click the FS1132.exe file from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe is used.

168/90x Licensing

The FS4400 Protocol Decoder is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading configuration files

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Configuration Files

The analyzers supported by the FS4400 configuration files are for the 16717 or better on the 16700/702 frames. 16753 and better analyzer cards are recommended.

167xx Analyzer	169xx Analyzer	X1 Mode using FS1033 cable 1 way	X1 Mode using FS1033 cable 2 way	X1 Mode using FS1034 cable 1 way	X1 Mode using FS1034 cable 2 way	X2 or X4 Mode using FS1031 cable 1 way	X2 or X4 Mode using FS1031 cable 2 way	X2 or X4 Mode using FS1035 cable 1 way	X2 or X4 Mode using FS1035 cable 2 way
16715/6/7 or 16750-2		PE440_1	load twice	PE440_1	load twice	PE440_2	load twice	PE440_2	load twice
	16750-2, 16910/1	PE440_9	PE440_10	PE440_9	PE440_11	PE440_12	PE440_13	PE440_12	PE440_14
16753-6		PE440_5	load twice	PE440_5	load twice	PE440_5	load twice	PE440_5	load twice
	16753-6 or 1695x	PE440_15	PE440_16	PE440_15	PE440_17	PE440_15	PE440_16	PE440_15	PE440_17
16760		PE440_3	load twice	PE440_3	load twice	N/A		N/A	
	16760	PE440_20	PE440_21	PE440_20	PE440_22	N/A		N/A	
16740-2		PE440_1	load twice	PE440_1	load twice	N/A		N/A	
	16740-2	PE440_9	PE440_10	PE440_9	PE440_11	N/A		N/A	
1680x		PE440_54	PE440_50	PE440_54	PE440_51	PE440_54	PE440_50	PE440_54	PE440_51
1680/90 (Standalone)		PE440_23	PE440_24	PE440_23	PE440_25	N/A		N/A	

PE440_1 – 1 way consists of 1 logic analyzer card.

PE440_2* – 2 way consists of 2 separate logic analyzer cards.

PE440_3 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE440_5 – 1 way consists of 1 logic analyzer card.

PE440_9 – 1 way consists of 1 logic analyzer card.

PE440_10 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE440_11 – 2 way consists of a total of 4 logic analyzer cards, each analyzer consists of 2 logic analyzer cards configured as 1 machine in turbo mode.

PE440_12 – 1 way consists of consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE440_13 - 2 way consists of a total of 4 logic analyzer cards, each analyzer consists of 2 logic analyzer cards configured as 1 machine in turbo mode.

PE440_14 – 2 way consists of a total of 4 logic analyzer cards, each analyzer consists of 2 logic analyzer cards configured as 1 machine in turbo mode.

PE440_15 – 1 way consists of 1 logic analyzer card.

PE440_16 – 2 way consists of 2 separate logic analyzer cards.

PE440_17 – 2 way consists of 2 separate logic analyzer cards.

PE440_20 – 1 way consists of 2 logic analyzer cards configured as 1 machine.

PE440_21 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer.

PE440_22 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer.

PE440_23 – 1 way, 1680/90 Analyzer, Pods 1, 2, 3 and 4.

PE440_24 – 2 way, 1680/90 Analyzer, Pods 1 thru 8.

PE440_25 – 2 way, 1680/90 Analyzer, Pods 1 thru 8.

PE440_50 – 2 way, 1680x Analyzer, FS1031 or FS1033 cables

PE440_51 – 2 way, 1680x Analyzer, FS1034 or FS1035 cables

PE440_54 – 1 way, 1680x Analyzer, FS1034 or FS1035 cables

***** When loading these configurations in the 167xx frame please select the system configuration (file name without the letter appended).

X8 Configuration Files

167xx Analyzer	169xx Analyzer	X8 Mode using FS1037 cable		X8 Mode using FS1038 cable		X8 Mode using FS1039 cable	
		1 way	2 way	1 way	2 way	1 way	2 way
16715/6/7 or 16750/1/2		PE440_4	load twice	PE440_4	load twice	PE440_4	load twice
	1675x, 16910/1	PE440_29	PE440_28	PE440_29	PE440_30	PE440_29	PE440_30
16753-6		PE440_6	load twice	PE440_6	load twice	PE440_6	load twice
	16753-6 or 1695x	PE440_27	PE440_26	PE440_27	PE440_31	PE440_27	PE440_31
16760		N/A		N/A		N/A	
	16760	N/A		N/A		N/A	
16740/1/2		N/A		N/A		N/A	
	16740/1/2	N/A		N/A		N/A	
1680x		PE440_52	PE440_53	PE440_52	PE440_55	PE440_52	PE440_55

PE440_4* – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE440_6* – 2 way consists of 2 separate logic analyzer cards.

PE440_26 – 2 way, x8 link. 2 analyzers, 90 pin connector cards.

PE440_27 – 1 way, x8 link. 1 analyzer, 90 pin connector cards.

PE440_28 – 2 way, x8 link. 2 analyzers, 40 pin connector cards.

PE440_29 – 1 way, x8 link. 2 analyzers, 40 pin connector cards.

PE440_30 – 2 way, x8 link. 2 analyzers, 40 pin connector cards.

PE440_31 – 2 way, x8 link. 2 analyzers, 90 pin connector cards.

PE440_52 – 1 way, x8 link. 1680x analyzer

PE440_53 – 2 way, x8 link. 1680x analyzer, split machine.

PE440_55 – 2 way, x8 link. 1680x analyzer, split machine.

***** When loading these configurations in the 167xx frame please select the system configuration (file name without the letter appended).

10b Mode Configuration Files

167xx Analyzer	PCIe x1 10b mode	PCIe x2,x4 10b mode	PCIe x8 10b mode
16717/8/9, 16750/1/2	PE10b_1	PE10b_2	PE10b_3
16753/4/5/6	PE10b_4	PE10b_5	PE10b_6
16760	PE10b_7	PE10b_8	N/A
16740/1/2	N/A	N/A	N/A

FS4400 PCIe 10b Mode For 16700 Frame

PE10b_1 – 1 way consists of 1 logic analyzer card.

PE10b_2 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_3 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_4 – 1 way consists of 1 logic analyzer card.

PE10b_5 – 1 way consists of 1 logic analyzer card.

PE10b_6 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer.

PE10b_7 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer.

PE10b_8 – 1 way consists of 3 logic analyzer cards configured as 1 analyzer running in turbo mode.

10b Mode Configuration Files

169xx Analyzer	PCIe x1 10b mode		PCIe x2,x4 10b mode		PCIe x8 10b mode	
	1 way	2 way	1 way	2 way	1 way	2 way
16750/1/2, 16910/1	PE10b_1	PE10b_2	PE10b_3	PE10b_4	PE10b_5	PE10b_6
16753/4/5/6 1695x	PE10b_7	PE10b_8	PE10b_9	PE10b_10	PE10b_11	PE10b_12
16760	PE10b_13	load twice	PE10b_14	load twice	N/A	
16740/1/2	N/A	N/A	N/A	N/A	N/A	
1680/90	N/A	N/A	N/A	N/A	N/A	
1680x	PE10b_50	PE10b_51	PE10b_52	PE10b_53	PE10b_54	PE10b_55

FS4400 PCIe 10b Mode For 16900 Frame

PE10b_1 – 1 way consists of 1 logic analyzer card running in turbo mode.

PE10b_2 – 2 way consists of 2 separate logic analyzer cards running in turbo mode.

PE10b_3 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_4 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_5 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_6 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_7 – 1 way consists of 1 logic analyzer card.

PE10b_8 – 2 way consists of 2 separate logic analyzer cards.

PE10b_9 – 1 way consists of 1 logic analyzer card.

PE10b_10 – 2 way consists of 2 separate logic analyzer cards.

PE10b_11 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer.

PE10b_12 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer.

PE10b_13 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_14 – 1 way consists of 3 logic analyzer cards configured as 1 analyzer running in turbo mode.

PE10b_50 – 1 way consists of 17 channels.

PE10b_51 – 2 way consists of 34 channels.

PE10b_52 – 1 way consists of 68 channels.

PE10b_53 – 2 way consists of 128 channels.

PE10b_54 – 1 way consists of 102 channels.

PE10b_55 – 2 way consists of 204 channels.

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

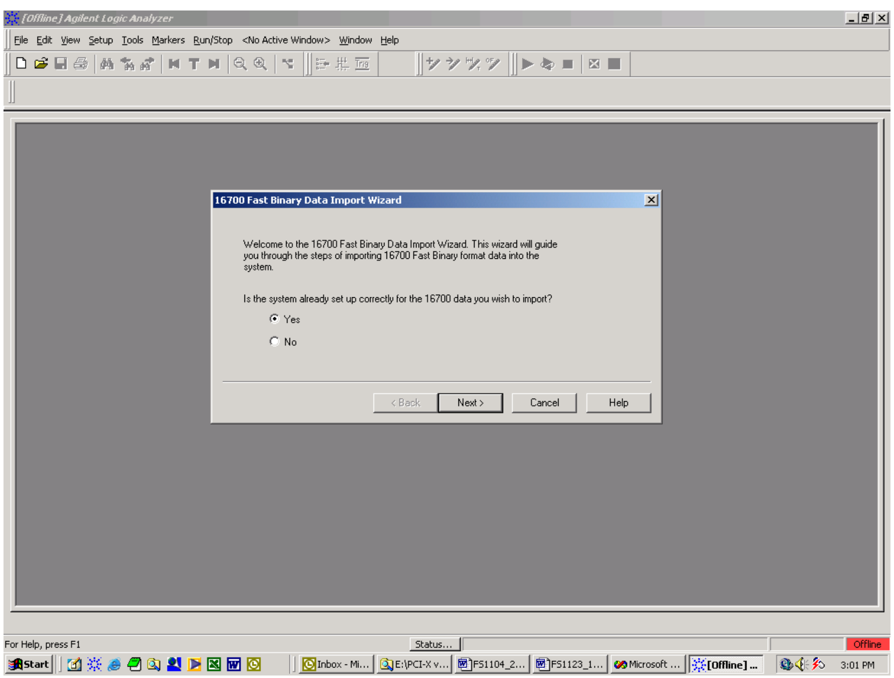
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may get additional licenses at no charge, please contact FuturePlus.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for “Setting up 1680/90/900 analyzer”. Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

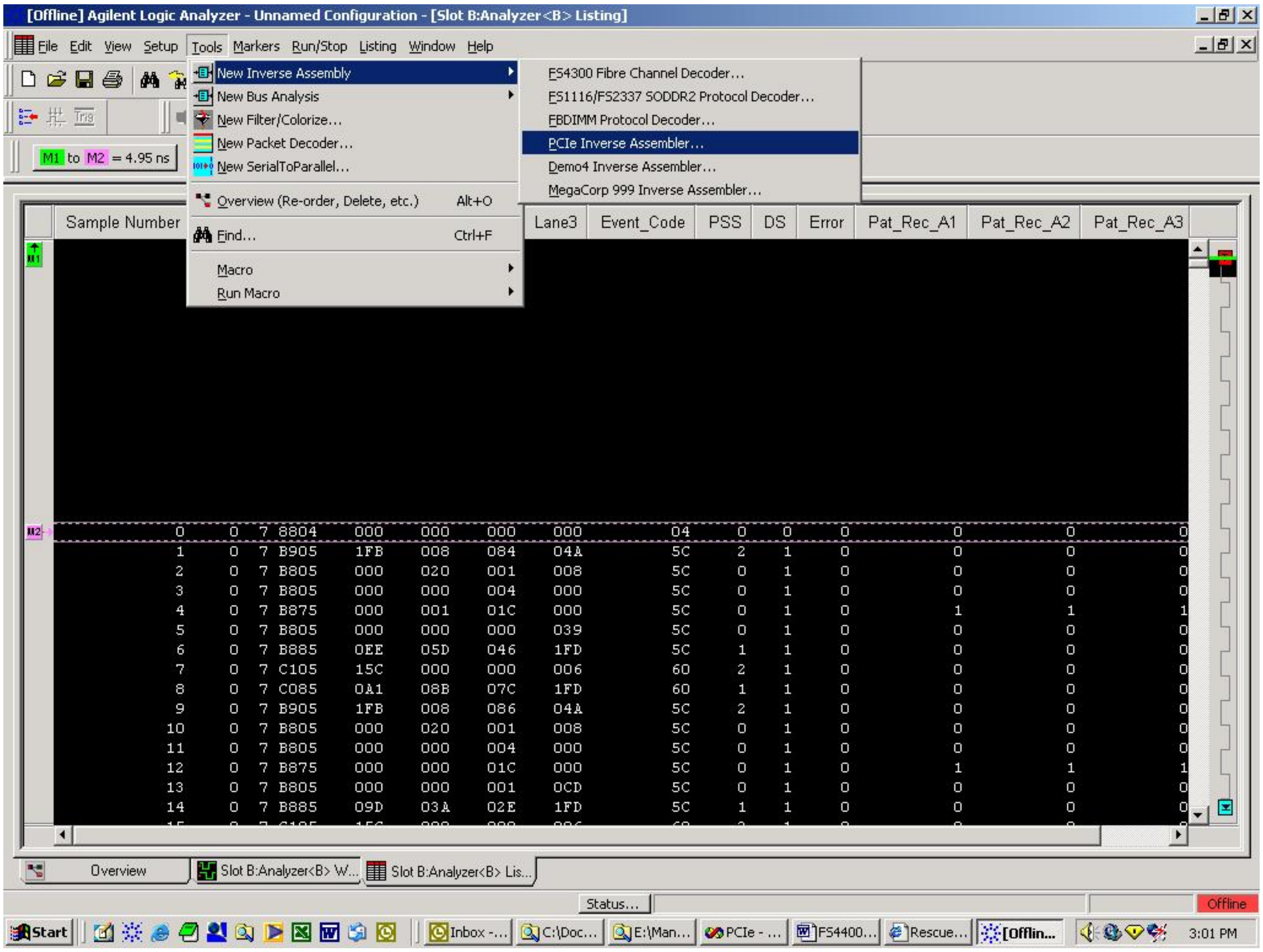
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select “yes” when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

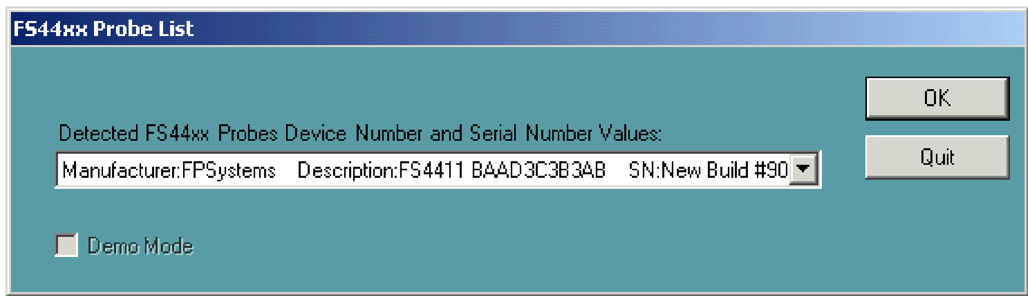
After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.



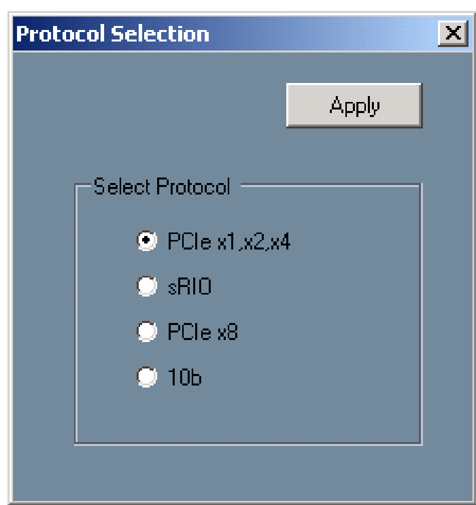
Probe Manager Application

The Probe Manager software can be found as the FS4400_probe_setup.exe file on the CD provided in the Documentation package. Insert the CD into the computer that will be used to control the FS4400 probe. This computer must have a USB connection. Using Windows File Manager, select the FS4400_probe_setup.exe file and double-click it, which initiates the installation software on the computer and places an icon on the desktop. Follow the directions that follow including agreeing to the license terms, once the software installation is complete click on finish. To start the program manager simply double click its desktop icon.

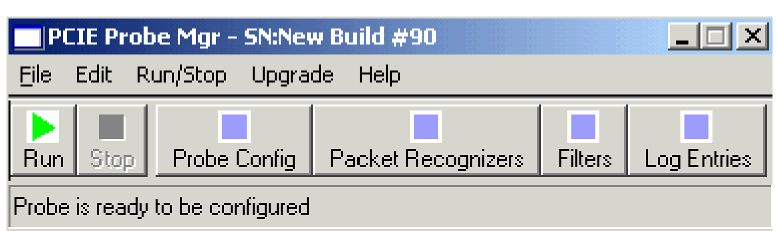
The Probe Manager application detects all FS44xx probes that are connected to the USB bus and allows the user to select which probe will be controlled by the current instance of the Probe Manager application from the initial screen as seen below.



The initial screen is followed by the Protocol Selection screen, in which the user selects the protocol the FS4400 probe will be associated with.



Once the protocol has been selected, the application displays the Main dialog as seen below:



The user configures and controls the probe from the main form. The form is composed of a menu bar, a tool bar and a status message bar. The menu bar provides options that allow the user to configure and run the probe. The tool bar provides options to configure the probe and the status bar displays the probes current status and/or any errors that may have been encountered. Error messages displayed in the status bar are also logged in the Log Form if logging is enabled.

The menu bar contains the following options:

File

- Open Config File – Displays a open file dialog in which the user may navigate to and open the file contains a previous session's saved probed settings.
- Save As - Displays a save file dialog in which the user may specify where a probe settings configuration file may be saved.
- Exit – Shut down the application.

Edit

- Modify Title String – Allows the user to specify the title string that appears in all sub-dialog's title bar. This is helpful when running multiple probes.

Run/Stop

- Run Probe Mgr – Running the probe with the current settings. This is an alternative to clicking the tool bar Run button.
- Stop Probe Mgr - Stop the probe. This is an alternative to clicking the tool bar Stop button

Upgrade

- Upgrade – Upgrade one of four protocol specific FPAG configurations.

Help

- About – Display version numbers for the Probe Manager application and FPGA configuration.

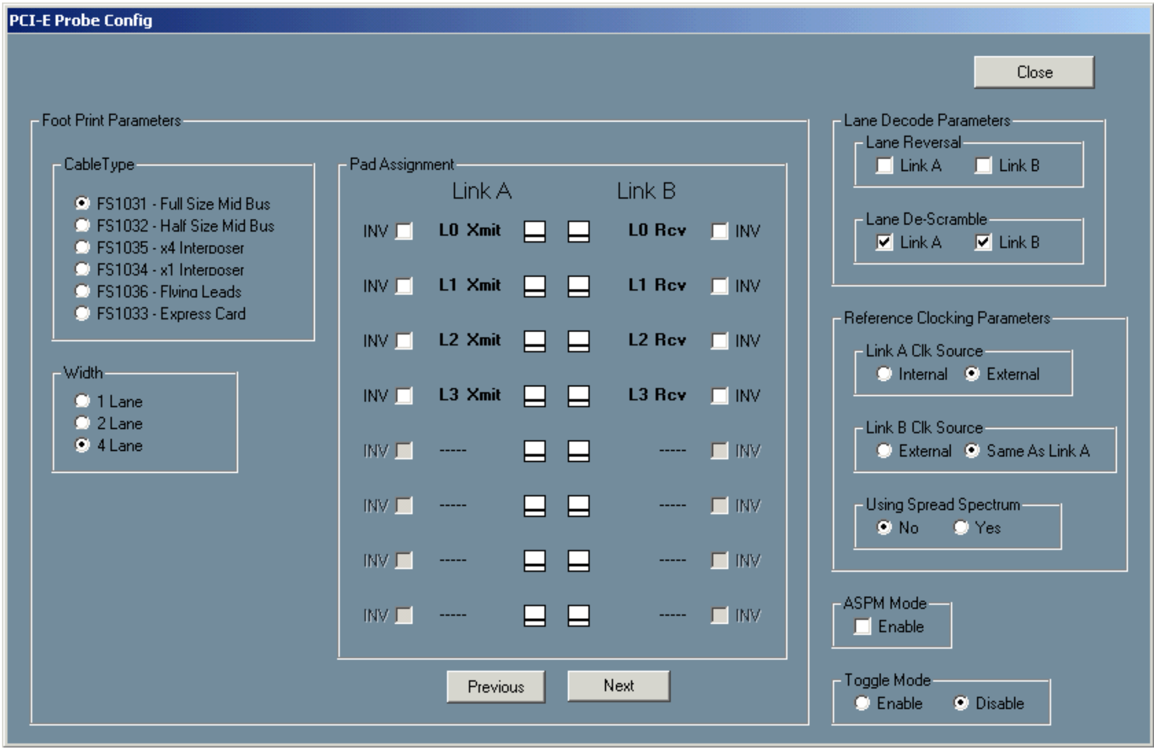
The application displays up to five sub-dialogs in a modeless manner. The sub-dialogs are used to configure the FS4400 probe.

The five sub-dialogs are:

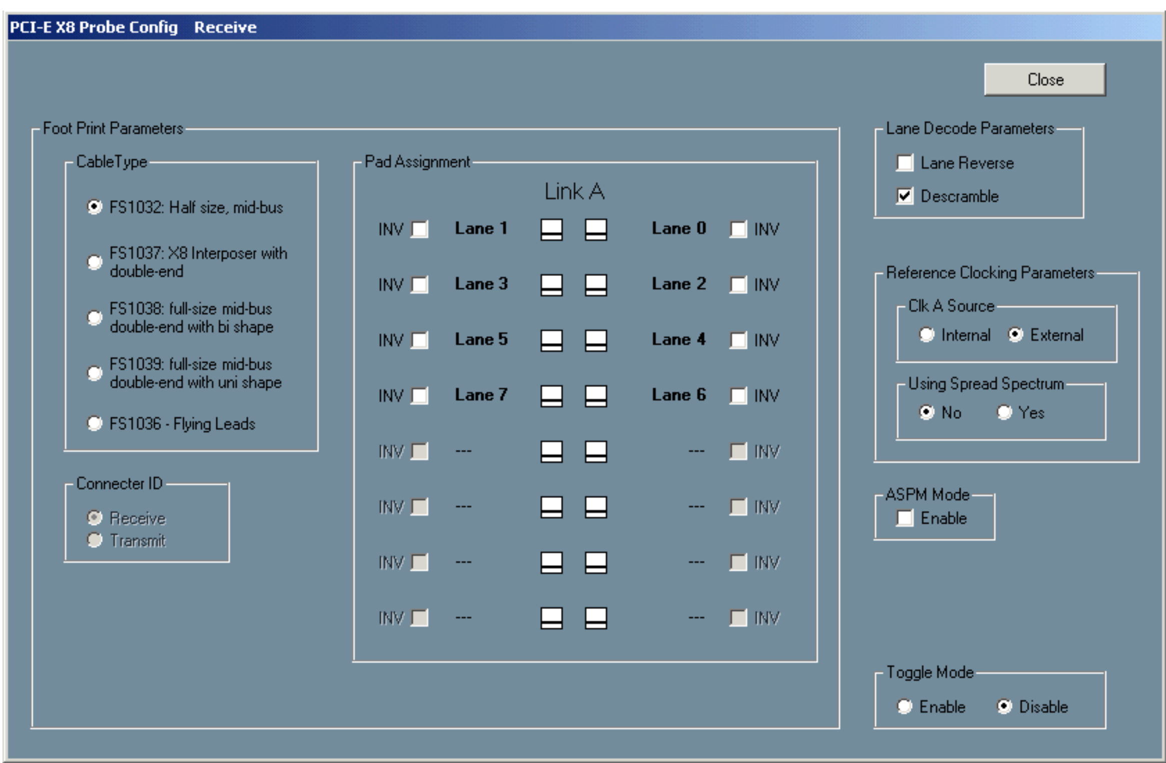
- Probe Configuration – Covers the type of probe cable used and basic aspects of the link being probed.
- Packet Recognizers – Set up the 3 Packet Recognizers provided per Link, which may be used to specify packet header based triggering parameters.
- Filters – Allows the user to specify the types of packets to be filtered
- Log Entries – Run time probe status.

Probe Configuration

The Probe Configuration dialog provides the user with ability to configure the probe and monitor signal activity on each channel.



-Probe Config X1 X2 X4 Dialog



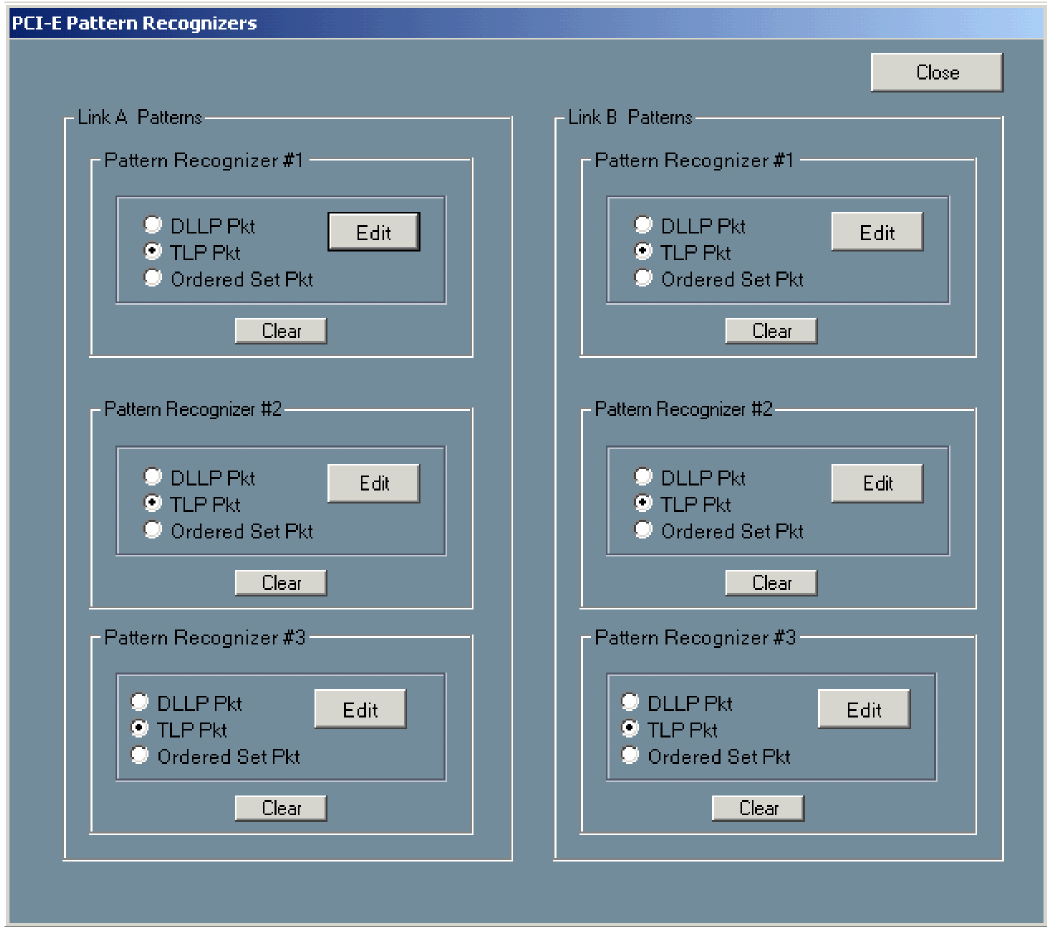
Probe Config X8 Dialog

The functions provided on these forms include:

- Selection of the Probing Cable type, Link width, and pad arrangement (referring to the arrangement of lanes on the mid-bus probe pads; see the “PCI Express Probing Design Guide for the FS4400” for more specific information).
- The Pad Assignment graphic shows the assignment of logical lanes as a result of user selections, and also represents the physical layout of mid-bus pads. The FS4400 processes channels from the left column in link-processor A and from the right column in link-processor B.
- Next or Previous buttons scroll through the various types of currently supported pad assignments (see the “PCI Express Probing Design Guide for the FS4400” for details of supported pad assignments).
- Lane Inversion can be selected on an individual channel basis by clicking the INV button associated with each lane.
- While the probe is stopped, signal activity indicators are provided on each channel. Signal presence is indicated by an up-down arrow symbol and a lack of signal presence is indicated by a flat horizontal line symbol.
- Selection of Lane Reversal on each link.
- Selection of Data Descrambling on each link.
- Reference Clocking choices are to use the FS4400 Internal reference on both links (these links must have 100 PPM frequency accuracy) or use External Reference Clock signal(s) from the target platform, via the FS4400 external Ref. Clock cable. For PCIe, the expected frequency is 100 MHz. If necessary, PCIe probing with a 125 MHz reference clock is supported by the FS4400, contact FuturePlus Systems for details.
- Selection of external reference clock source for link B: same as A (common clock, uses the Reference Clock A probe input), or different (distinct clock, uses Reference Clock B probe input).
- Selection of Spread Spectrum clock processing mode. Activate only when spread spectrum modulation is in use (requires external reference clock).
- Selection of Active-State Power Management (ASPM) mode. Activate when the target link state is repeatedly switching between normal operational (L0) and shallow power saving (L0s) states. Activating this control allows the probe hardware to decode traffic starting early in the Fast Training process, usually within the first few FTS Ordered Sets transmitted when the link returns to L0 state. Activating this control comes with a small price in that LOS status for the active lanes is not available while the probe is running. There are two consequences of running in ASPM mode:
    - Signal loss is reported on LEDs and in the Log File as other types of errors (that result from signal loss).
    - LOS status bits can not be used for triggering the logic analyzer, and are not useful in the listing, because they are forced to 0 (only while running and only on active lanes).
- Selection of Toggle mode. When activated, the probe output signals to the logic analyzer pods and the link status LEDs are toggled.

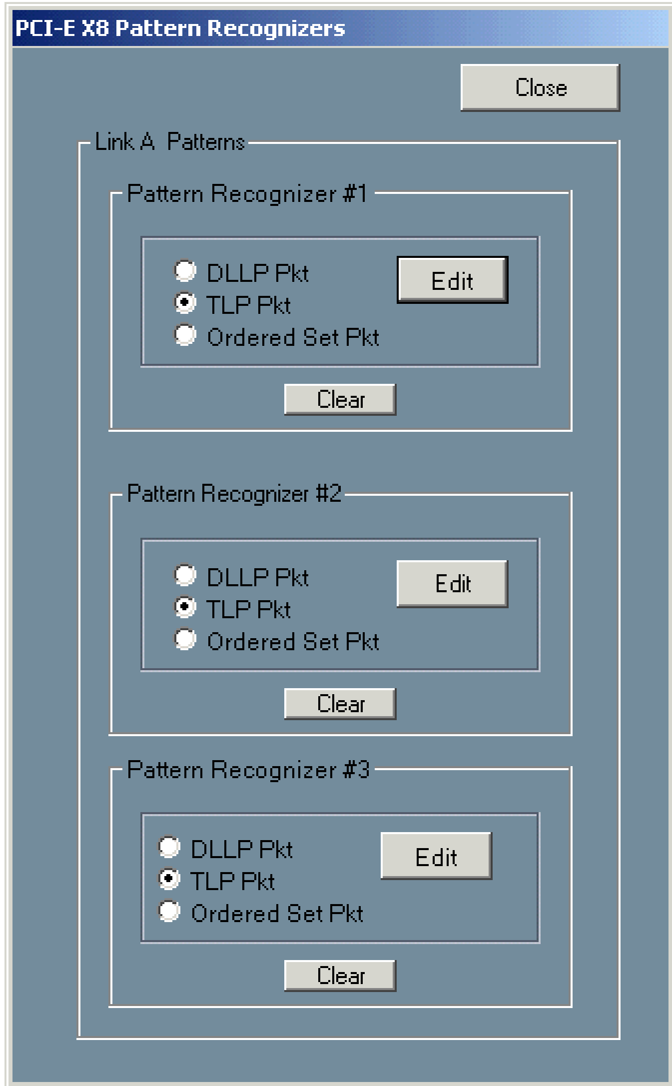
Packet Recognizers

This dialog form provides the ability to setup the three 24-byte Pattern Recognizers provided on each link.



Pattern and Mask X1,X2,X4 Dialog

Because the pattern recognizers look at the first 24 bytes of each packet (or ordered set), they are also referred to as packet recognizers.

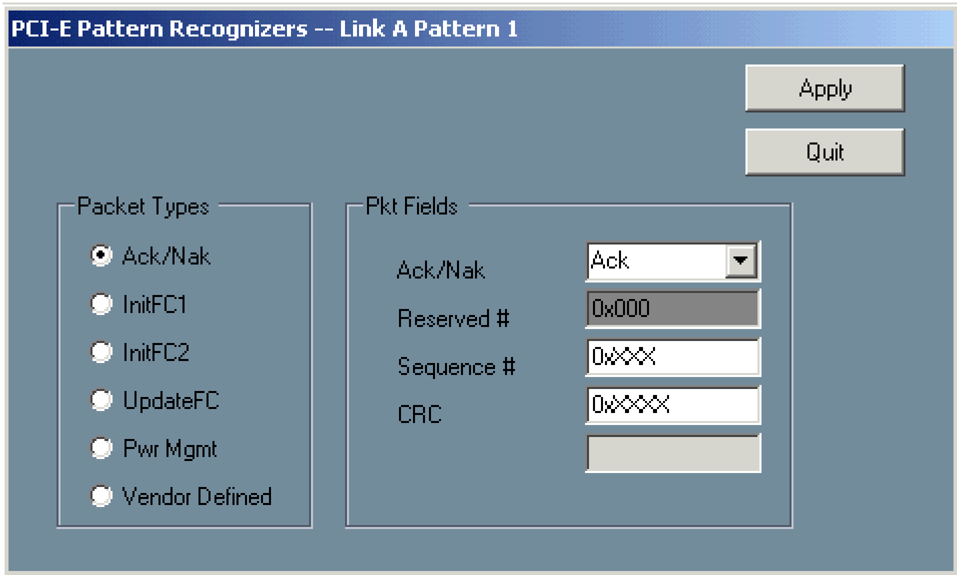


Pattern and Mask X8 Dialog

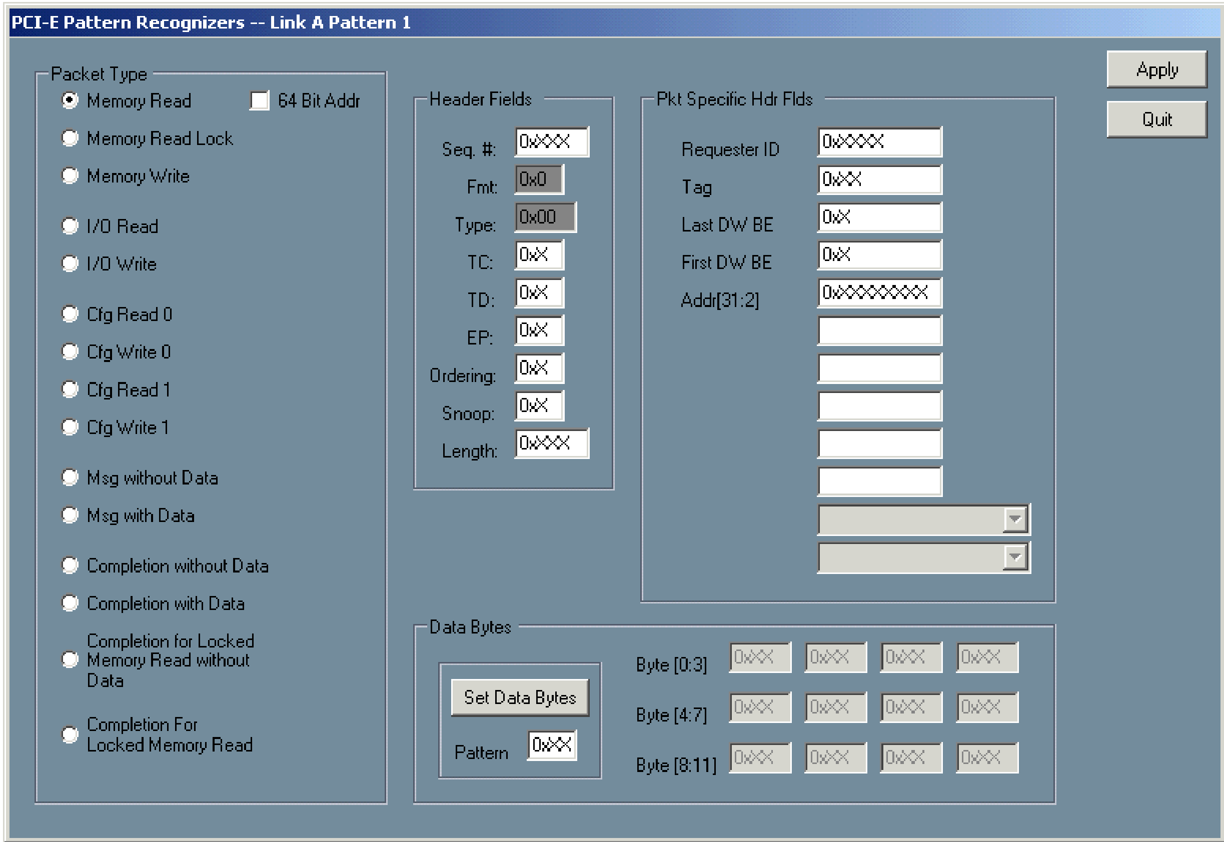
The Packet Recognizer dialog allows a user to specify the packet recognizer pattern.

The x1, x2 and x4 Packet Recognizer dialog allows the user to enter up to 6 patterns (3 on link A and 3 on link B). In x8 mode, the user can enter up to 3 patterns. In x8 mode, packets are detected if they start on lane 0 or lane 4.

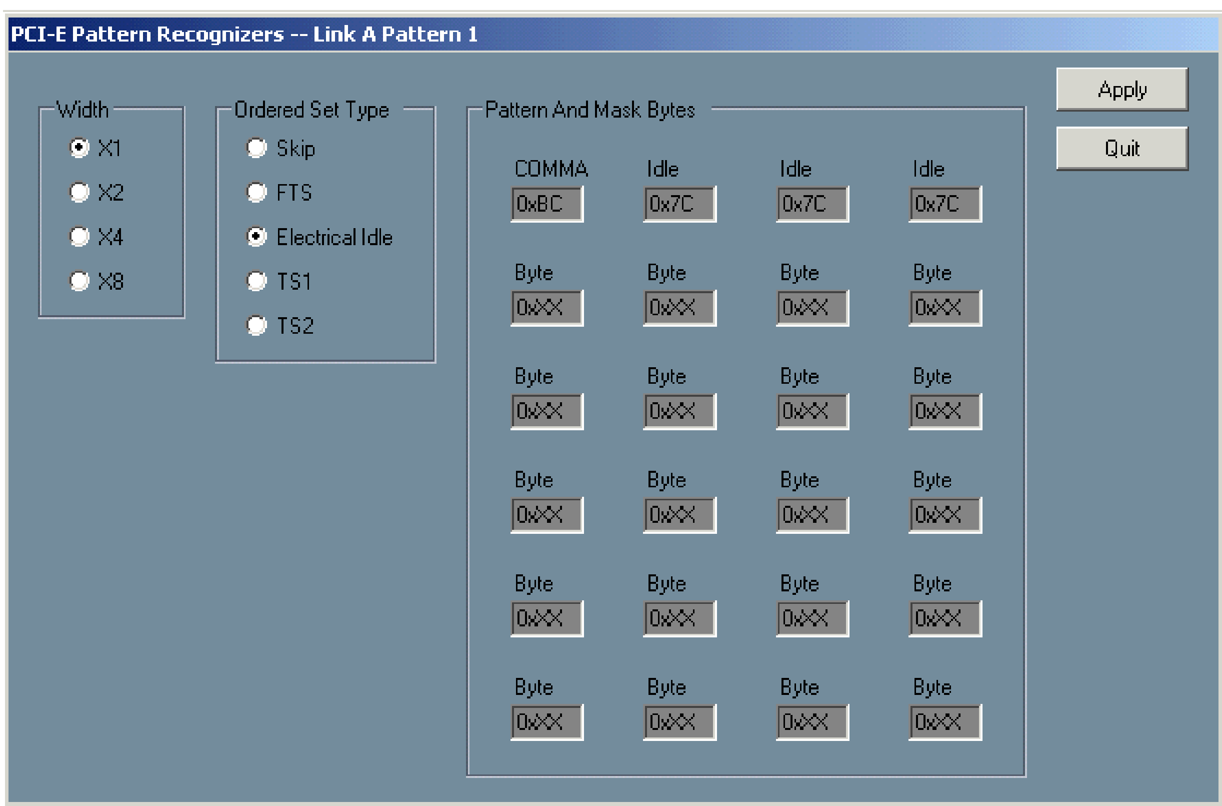
The pattern is entered via a sub-dialog that is displayed after the user has clicked one of the six Edit buttons. There are three sub-dialog forms, one for Ordered Sets, one for DLLP packets, and one for TLP packets as shown below.



DLLP Pattern and Mask Dialog



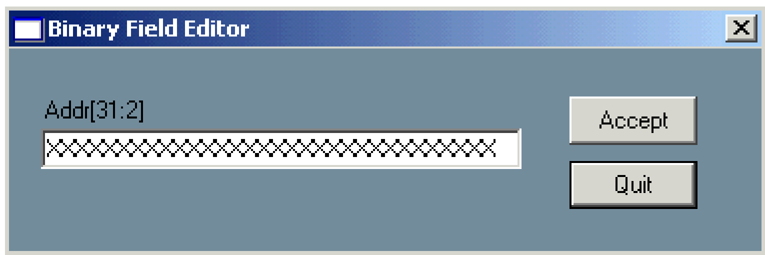
TLP Pattern and Mask Dialog



Ordered Set Pattern and Mask Dialog

The DLLP, TLP and Ordered Set sub-dialog screens are designed such that the minimum numbers of fields are specified to form a valid packet. Fields displaying X's will be masked out. All reserved fields will be masked into the pattern.

Every field is validated as the user is entering the hex values. The user may enter any combination of X's and hex digits into each field. Each field may be edited in binary form by right clicking the mouse key, at which point the contents of the field are displayed in binary format in a separate window. When the user applies the binary values (by clicking the Accept button), the binary value is converted to a hex representation and displayed in the pattern dialog. Field Hex digits that are partially masked will be displayed with a "$" character.



Binary Editor Dialog

The packet recognition setups are created via sub-dialogs that are displayed whenever the user selects a packet type (via the radio buttons for each link pattern) and clicks the Edit button.

The pattern is edited if the user clicks the Apply button on the packet-specific sub-dialogue form. If edited, the packet type string is displayed in a light blue color.

Once edited, the pattern may be cleared by clicking the Clear button. This will inactivate the recognizer.

Pattern Recognizers are used to trigger the logic analyzer whenever a specific packet or ordered set pattern is encountered. Each Pattern recognizer outputs a PAT_REC flag to the logic analyzer that pulses high during the 1st state of each packet.

Pattern recognizers may also be used as filters.

The Pattern Recognizer examines the first 24 bytes of each packet. Recognizers are setup by the Probe Manager with a match pattern and a separate mask pattern, giving the user control over the comparison, bit by bit.

The probe must be stopped before editing patterns.

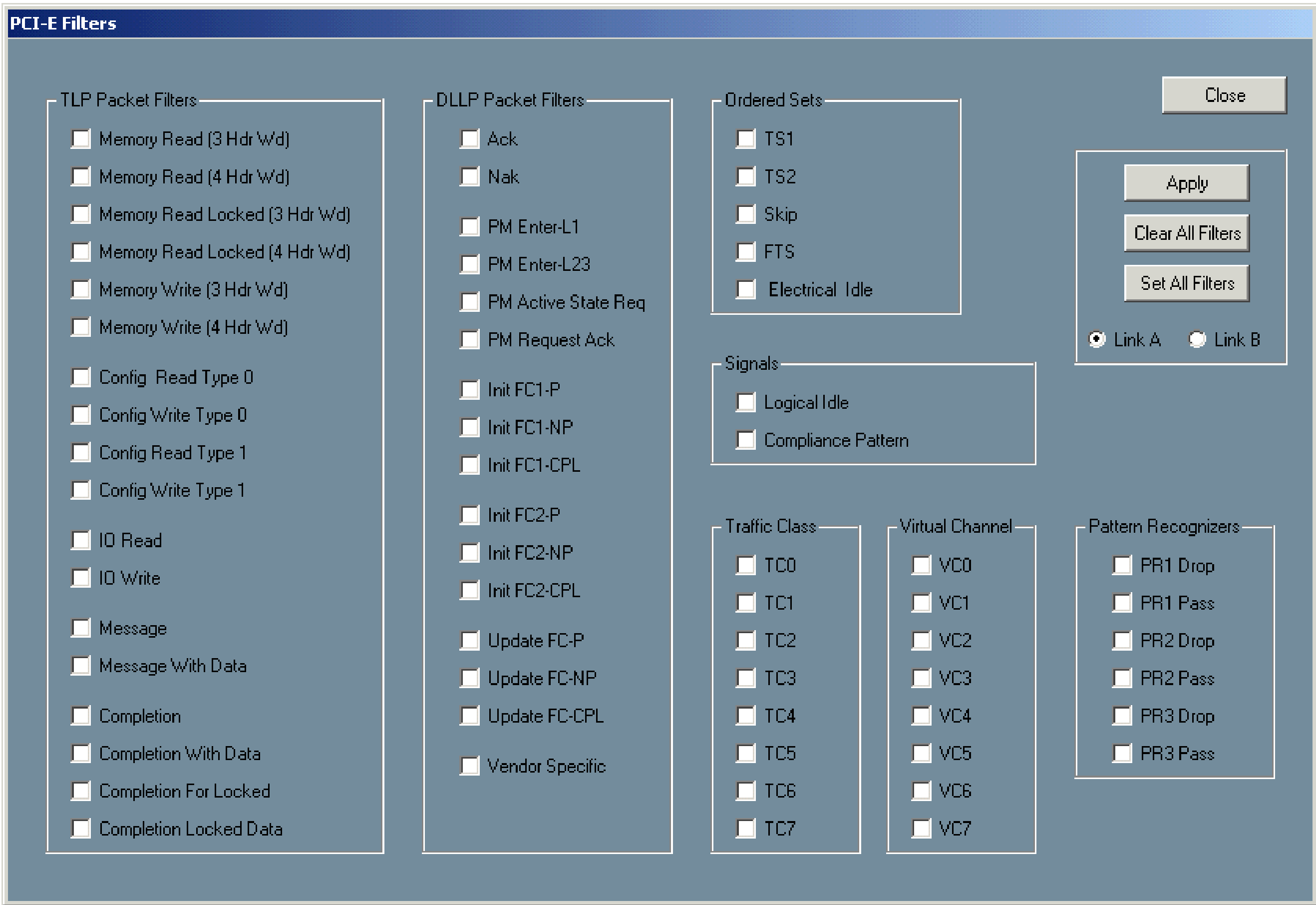
You must always restart the probe by pressing the green run button on the main window so the new values will be written to the probe hardware.

Filtering

The Filter dialogue page provides the user with a comprehensive suite of predefined filter functions to apply to either Link.

Filter types include all TLP and DLLP packets, Ordered Sets, Traffic Class, Virtual channel, and special signal states.

Additionally, filters are provided to Pass or Drop packets that have been recognized by the three packet recognizers.



Filters X1,X2,X4 Dialog

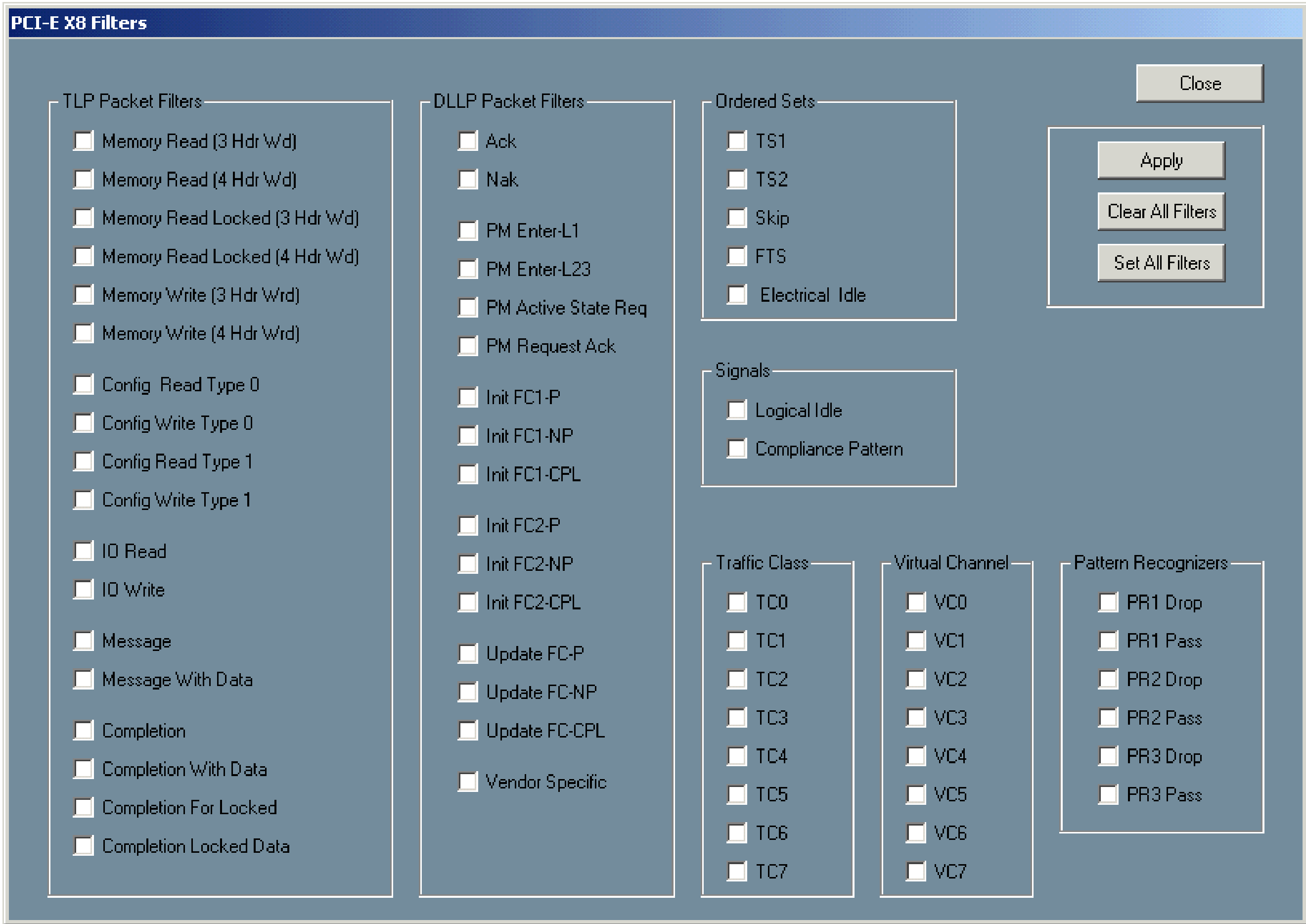
Filtering is done in real time by the FS4400 hardware.

Filtering out unwanted traffic such as Logical Idles can extend the storage capabilities of the logic analyzer. Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

To filter out any particular traffic type, click on the appropriate box so a √ appears and click apply. You must restart the probe by pressing the green run button so the new values will be written to the probe hardware.

Use Link A and Link B buttons to switch to the other link's filter.

Filtering can also be done using any combination of packet header bits, via the Pattern Recognizers. The "PR Drop" filters drop the recognized packets. The "PR Pass" filters over-ride all other filters, and force recognized packet to be clocked into the analyzer.



Filters X8 Dialog

Filtering is done in real time by the FS4400 hardware.

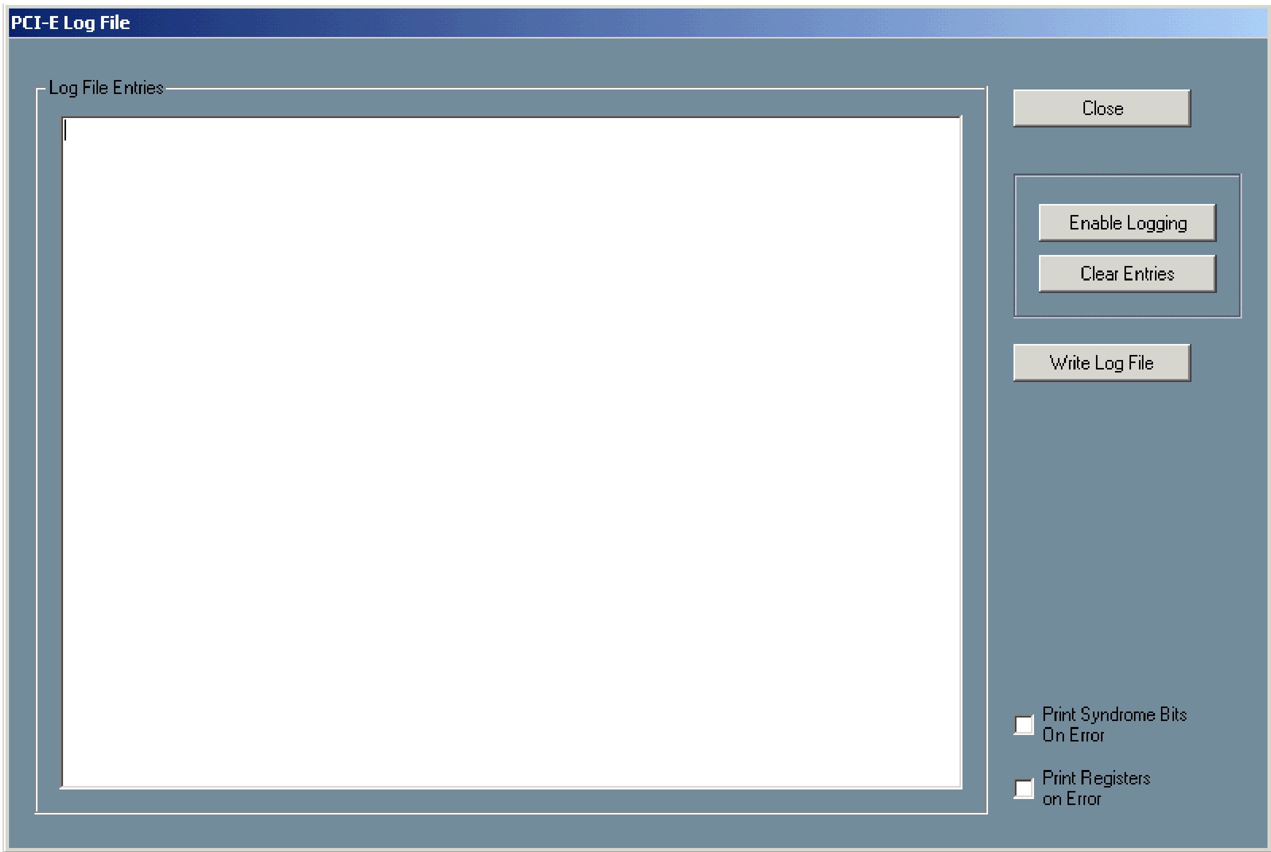
Filtering out unwanted traffic such as Logical Idles can extend the storage capabilities of the logic analyzer. Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

To filter out any particular traffic type, click on the appropriate box so a √ appears and click apply. You must restart the probe by pressing the green run button so the new values will be written to the probe hardware.

Filtering can also be done using any combination of packet header bits, via the Pattern Recognizers. The “PR Drop” filters drop the recognized packets. The “PR Pass” filters over-ride all other filters, and force recognized packet to be clocked into the analyzer.

Log File

The status of the probe, and the link under test, can be seen in this tab page.



Log File Dialog

Once started, logging continues even if the probe is stopped and started, or if the log window is closed and re-opened.

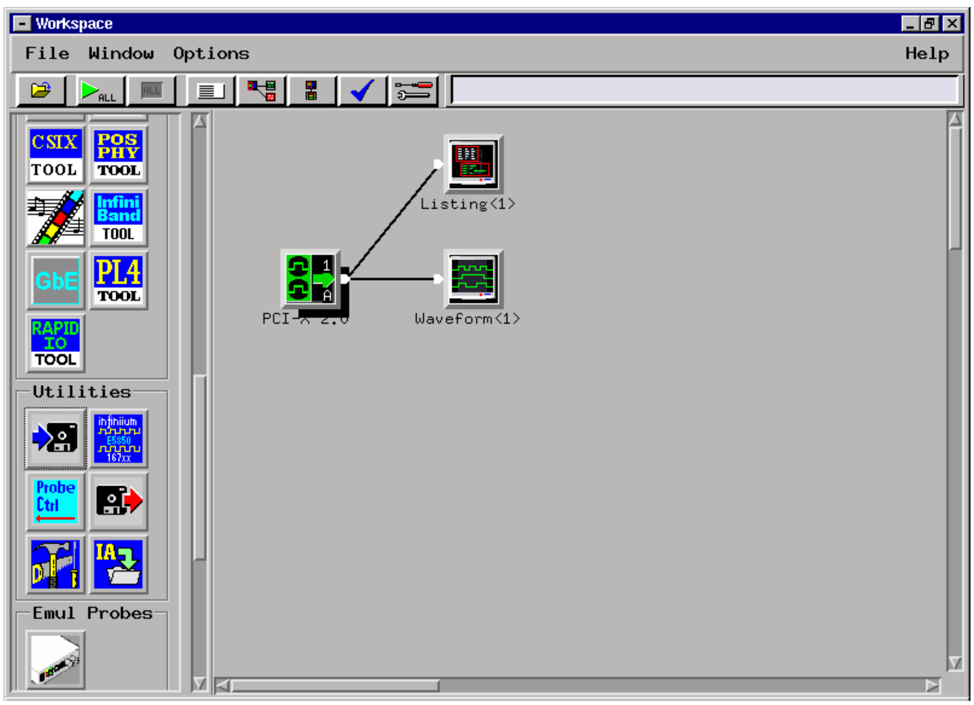
Once a probe has been stopped, the log entries can be written to a file of the user's choice by clicking the Write Log File button.

State Analysis

The PCI Express Protocol Decode Software

This chapter explains how to use the FS4400 to perform state analysis. The configuration file sets up the format specification menu of the logic analyzer for compatibility with the output of the FS4400.

Loading the configuration file will automatically load the PCI Express Protocol Decode software (FS4400) onto the workspace. If this does not happen then check to make sure that the PCI Express decode software was properly installed.



Labels (PCIe)

Besides de-serializing the data stream for the logic analyzer, the FS4400 generates a number of identification and control bits that are used by the Protocol Decoder and logic analyzer. These are also available to the user and can be used as described below.

Pre-defined Label	**No. of Bits**	**Definition/Usage**	**Logic Analyzer Pod** **x1, x2, x4 mode**	**Logic Analyzer Pod** **x8 mode**
VAB		Collection of all flags for Inverse Assembler usage.		
DS (Default Store Flag)	1	1= Store this state 0 = Discard This signal must be used for default store qualification.	A4[16] (CLK)	B4[10] (CLK)
PSS (Packet Sample State)	2	PSS[1] = Start of Packet flag PSS[0] = End of Packet flag 10=start, 01=end, 11= start & end 00=inside packet, ordered set or idle. Use PSS[1] = 1 in conjunction with Event_Code to detect each occurrence.	A4[5:4]	B4[3:2]
Unjust	1	X8 only: When set, indicates a packet beginning at lane 4 rather than lane 0.	NA	B4[4]
Event_Code	6	Describes what type of packet, ordered set, signal event or error event. Code is held for duration of packet or ordered set, except that probe-generated signal and error events can over-write any state except the start state. When start and end coincide, the event code for the starting packet is displayed. See next page for a list of event code values.	A4[0:3], A3[16:15]	B4[1:0], B3[16:13]
Error	1	1= This state includes an error	A4[13]	B4[8]
Pat_Rec_3 Pat_Rec_2 Pat_Rec_1 (Pattern Recognizers)	3	1= Packet recognized (pulsed for one clock cycle). These are to be used for logic analyzer triggering only. Do not qualify with DS.	A4[11:9]	B4[7:5]
Lane0	10	Logical Lane 0 Data (spread data in x1 or x2 lane mode) Bit 9 is Invalid flag, Bit 8 is Control flag	A3[6:0],A2[16:14]	A2[16:7]
Lane1	10	Logical Lane 1 Data (spread data in x1 or x2 lane mode) Bit 9 is Invalid flag, Bit 8 is Control flag	A2[13:4]	A2[6:0], A1[16:14]
Lane2	10	Logical Lane 2 Data (spread data in x1 or x2 lane mode) Bit 9 is Invalid flag, Bit 8 is Control flag	A2[3:0],A1[15:10]	A1[13:4]
Lane3	10	Logical Lane 3 Data (spread data in x1 or x2 lane mode) Bit 9 is Invalid flag, Bit 8 is Control flag	A1[9:0]	A1[3:0], B4[16:11]

Lane 4	10	Logical Lane 4 Data (x8 mode only) Bit 9 is Invalid flag, Bit 8 is Control flag	NA	B3[11:2]
Lane 5	10	Logical Lane 5 Data (x8 mode only) Bit 9 is Invalid flag, Bit 8 is Control flag	NA	B3[1:0], B2[16:9]
Lane 6	10	Logical Lane 6 Data (x8 mode only) Bit 9 is Invalid flag, Bit 8 is Control flag	NA	B2[8:0], B1[15]
Lane 7	10	Logical Lane 7 Data (x8 mode only) Bit 9 is Invalid flag, Bit 8 is Control flag	NA	B1[14:5]

Additional Bits (PCIe)

The FS4400 generates a number of identification and control bits that are used by the Protocol Decoder and logic analyzer. There are a few that don't have pre-defined labels, (other than being in the VAB label used by the Inverse Assembler).

These are also available to the user and can be used as described below.

Functional Name	**No. of Bits**	**Definition/Usage**	**Logic Analyzer Pod** In x1 x2 x4 mode	**Logic Analyzer Pod** In x8 mode
ALIGNED	1	1 = multi-lane link is aligned 0 = lane deskew has failed	A4[14]	B4[9]
DATA PRESENT [3,2,1,0]	4	(Exists in x1 x2 x4 mode only.) 1 = Lane data is present. 0 = Lane data is not present due to effects of spreading x1 or x2 data across 4 lanes.	A3[14:11]	NA
LOS [3,2,1,0]	4	Lane-by Lane LOS bits. (Provided in x1 x2 x4 mode only.) 1 = Loss of Signal in Lane 0 = Signal Detected or Lane not used	A3[10:7]	NA
Any LOS	1	Composite LOS bit (all active lanes) (Provided in x8 mode only.)	NA	B3[12]

Event Code label definitions (PCIe mode):

Event		Event code
Unknown (loss of frame synch)		0x00
Electrical Idle Signal Event		0x01
Beacon Signal Event		0x02
Link Alive Signal Event		0x03
Signal Logical Idle		0x04
Signal Compliance Pattern		0x0C
Ordered Set TS1		0x05
Ordered Set TS2		0x06
Ordered Set Skip		0x07
Ordered Set FTS		0x08
Ordered Set Electrical Idle		0x09
TLP Memory Read	MRd	0x10
TLP Memory Read Locked	MRdLk	0x11
TLP Memory Write	MWr	0x12
TLP IO Read Request	IORd	0x13
TLP IO Write Request	IOWr	0x14
TLP Config Read Type 0	CfgRd0	0x15
TLP Config Write Type 0	CfgWr0	0x16
TLP Config Read Type 1	CfgRd1	0x17
TLP Config Write Type 1	CfgWr1	0x18
TLP Message	Msg	0x19
TLP Message with Data	MsgD	0x1A
TLP Completion	Cpl	0x1B
TLP Completion with Data	CplD	0x1C
TLP Completion for Locked	CplLk	0x1D
TLP Completion Locked Data	CplDLk	0x1E
DLLP Ack		0x20
DLLP Nak		0x21
DLLP PM-Enter-L1		0x22
DLLP PM-Enter-L23		0x23
DLLP PM-Active-State-Req		0x24
DLLP PM-Request-Ack		0x25
DLLP Vendor-specific		0x26
DLLP InitFC1-P		0x27
DLLP InitFC1-NP		0x28
DLLP InitFC1-CPL		0x29
DLLP InitFC2-P		0x2A
DLLP InitFC2-NP		0x2B
DLLP InitFC2-CPL		0x2C
DLLP UpdateFC-P		0x2D
DLLP UpdateFC-NP		0x2E
DLLP UpdateFC-Cpl		0x2F
Error Unexpected K		0x30
Error Packet Ends Bad		0x31
Link Down Signal Event		0x33
Error Logical Idle		0x34
Error Invalid Symbol Decode		0x35
Error Unexpected LOS		0x36
Error Framing		0x37
Error Alignment (X8 mode only)		0x38
Error Control Column (X8 mode only)		0x39
Error TSID (X8 mode only)		0x3A
Error TLP Decode (X8 mode only)		0x3D
Error DLLP Decode (X8 mode only)		0x3E

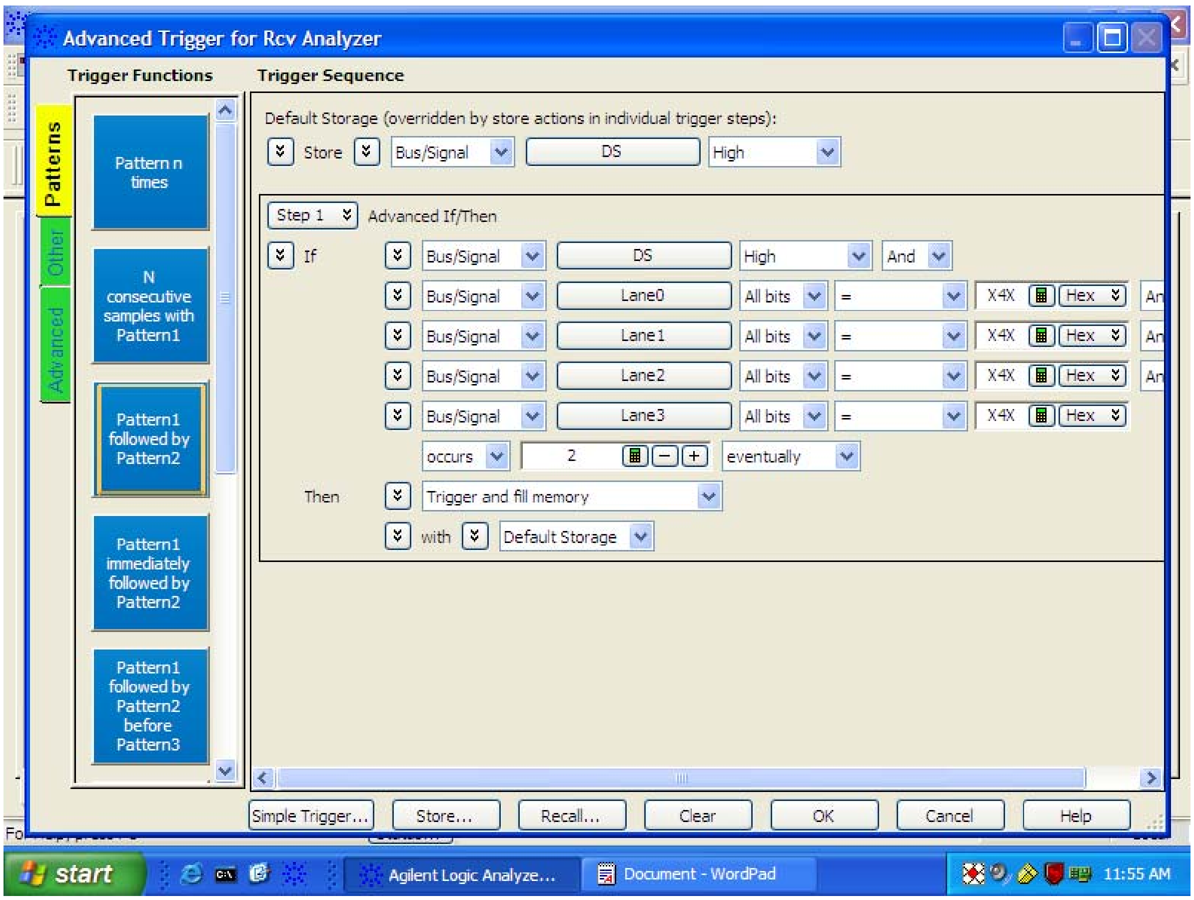
Labels (10b)

Besides de-serializing the data stream for the logic analyzer, the FS4400 in 10b Mode generates a number of status bits that are available to the user and can be used for triggering and analysis as described below.

Pre-defined Label	**No. of Bits**	**Definition/Usage**	**Logic Analyzer Pod** **10-bit, x1 mode** (use B pods for other link)	**Logic Analyzer Pod** **10-bit, x2, x4 mode** (use B pods for other link)	**Logic Analyzer Pod** **10-bit, x8 mode**
Align Flag	1	1= Alignment of multi-lane link detected	NA	A4[4]	A2[15]
Any Invalid Error Flag	1	1= This state includes an 8b10b code error (either disparity error or decode error in any active lane)	A1[0]	A4[3]	A2[14]
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect on lane (x2 x4 mode only)	NA	A4[2:0] A3[16]	NA
Any LOS	1	1= Loss of Signal detected in any active lane 0= Signal detected in all active lanes	A1[15]	A3[15]	A2[13]
Lane 0 Disparity Error	1	1= Lane 0 data has incorrect 8b10b disparity	A1[14]	A3[14]	A2[12]
Lane 0 Invalid Decode Error	1	1= Lane 0 data is not a valid 8b10b code	A1[13]	A3[13]	A2[11]
Lane0	10	Physical Lane 0 Data, 10-bit encoded	A1[12:3]	A3[12:3]	A2[10:1]
Lane 1 Disparity Error	1	1= Lane 1 data has incorrect 8b10b disparity	NA	A3[2]	A2[0]
Lane 1 Invalid Decode Error	1	1= Lane 1 data is not a valid 8b10b code	NA	A3[1]	A1[15]
Lane1	10	Physical Lane 1 Data, 10-bit encoded	NA	A3[0] A2[16:8]	A1[14:5]
Lane 2 Disparity Error	1	1= Lane 2 data has incorrect 8b10b disparity	NA	A2[7]	A1[4]
Lane 2 Invalid Decode Error	1	1= Lane 2 data is not a valid 8b10b code	NA	A2[6]	A1[3]
Lane2	10	Physical Lane 2 Data, 10-bit encoded	NA	A2[5:0] A1[15:12]	A1[2:0] B4[16:10]
Lane 3 Disparity Error	1	1= Lane 3 data has incorrect 8b10b disparity	NA	A1[11]	B4[9]
Lane 3 Invalid Decode Error	1	1= Lane 3 data is not a valid 8b10b code	NA	A1[10]	B4[8]
Lane3	10	Physical Lane 3 Data, 10-bit encoded	NA	A1[9:0]	B4[7:0] B3[16:15]
Lane 4 Disparity Error	1	1= Lane 4 data has incorrect 8b10b disparity	NA	NA	B3[14]
Lane 4 Invalid Decode Error	1	1= Lane 4 data is not a valid 8b10b code	NA	NA	B3[13]
Lane4	10	Physical Lane 4 Data, 10-bit encoded (x8 mode only)	NA	NA	B3[12:3]
Lane 5 Disparity Error	1	1= Lane 5 data has incorrect 8b10b disparity	NA	NA	B3[2]
Lane 5 Invalid Decode Error	1	1= Lane 5 data is not a valid 8b10b code	NA	NA	B3[1]
Lane5	10	Physical Lane 5 Data, 10-bit encoded (x8 mode only)	NA	NA	B3[0] B2[16:8]
Lane 6 Disparity Error	1	1= Lane 6 data has incorrect 8b10b disparity	NA	NA	B2[7]
Lane 6 Invalid Decode Error	1	1= Lane 6 data is not a valid 8b10b code	NA	NA	B2[6]
Lane6	10	Physical Lane 6 Data, 10-bit encoded (x8 mode only)	NA	NA	B2[5:0] B1[15:12]
Lane 7 Disparity Error	1	1= Lane 7 data has incorrect 8b10b disparity	NA	NA	B1[11]
Lane 7 Invalid Decode Error	1	1= Lane 7 data is not a valid 8b10b code	NA	NA	B1[10]
Lane7	10	Physical Lane 7 Data, 10-bit encoded (x8 mode only)	NA	NA	B1[9:0]

Triggering

The configuration files provide some logic analyzer based trigger set-ups that utilize the pre defined symbols described earlier.



Remember to always use DS for default storage, and use default storage to fill memory.

The 6-bit probe-generated Event Code field makes it easy to trigger on particular packet types. When triggering on Event Code always qualify it with:

- DS =1 (Already included in pre-defined Event Code symbol definitions)
- PSS[1] =1 (The start of packet flag).

The probe-generated Packet Recognizer flags (Pat_Rec_3,2,1) make it easy to trigger on packets based on header or data bit patterns in the first 24 bytes of each packet. These flags are always valid, pulse once at the start of each recognized packet, and do not need any other bits to qualify them.

Acquiring Data

First, insure that the FS4400 probe is attached to its external power supply and powered on, which would be indicated by a green Power On LED. Open up the Probe Manager software and insure the appropriate selections are made and applied, finally make sure that the probe is connected via the appropriate cable(s) to the target system.

Once connected, with the link active, open up the Probe Config window and select cable type, lane width, and reference clock options. Verify that lane activity indicators show activity at the correct lanes. Run the probe and observe the LEDs.

If a link's Signal LED is green but its Data LED is orange then there may be a need to select different options for lane width, lane reverse or lane inversion in the Probe Config window.

The FS4400 probe should show a green Signal LED of any Link being probed, as well as a green or dark data LED.

Configure the analyzer trigger menu to acquire PCI Express data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE or when you select STOP.

The logic analyzer will flash "Slow or Missing Clock" if it does not see the signal CLK toggling.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

Link status is communicated by a pair of LEDs as follows:

Signal LED State	Meaning
Dark	LOS (no signal on an active lane)
Red	RX Fault: Lost Lock on Ref Clock, Lost Synch on Data, FIFO over run or under run. See Log for more information.
Orange	Invalid Symbol or Disparity Error
Green	OK

Data LED State	Meaning
Red	FPGA Lost lock on clock(s). Probe needs to stop and run again.
Orange	Any Error: Invalid Symbol or Disparity Error, Align, Framing, Idle.
Green	OK, Data clocking into analyzer.
Dark	No Data (due to filtering or not running)

All transient events such as a single bit error, or a packet clocked into the analyzer, are stretched to short visible pulses on the LEDs.

Observing Link Start-up:

When using Internal Reference clock, the probe can be run at any time, before or after the target has powered up or link become active.

When using External Reference clock(s), the probe requires the target reference clock to be active before the probe is run.

In all cases, links may be re-started, and target systems may be re-booted, while the probe is running. This makes probing link initialization convenient.

Observing PCIe Link Activity in ASPM :

PCI-Express Active State Power Management (ASPM) protocol, allows links to transition back and forth between active (L0) and low power states (L0s, L1, L2 etc).

The probe will follow links that go up and down:

- When a link is constantly transitioning back and forth between active and low power states, the Signal LEDs and the log file will report errors that can be ignored.
- The probe can follow Fast Training. If a link is transitioning between active (L0) and shallow power saving (L0s), the probe will achieve very low N_FTS when operated in ASPM mode, selected by clicking the “ASPM” checkbox on the Config window before running the probe. This mode allows the probe to start capturing data early during the Fast Training ordered sets.

Finding Stable PCIe Link Activity:

When a link is expected to perform initialization, set the analyzer to trigger on:

- “Event Code = TS2 training set”

This assures the link is up and running because a PCIe device issues TS2 ordered sets only after it has received valid TS1 ordered sets from the other direction.

Finding Link Startup During Fast Training:

When a link is expected to perform fast training, set the analyzer to trigger on:

- “Event Code = FTS Ordered Set”

Finding the Start of Signal Activity:

Set the analyzer to trigger on:

- “Event Code = Link Alive”

Another method is to trigger based on signal detection status (LOS = loss of signal). Note this method can only be used when the probe is not setup for ASPM mode:

- “Event Code = Beacon” (signal detected on lane 0)
- LOS[0] goes low (for 1-lane operation)
- LOS[1:0] goes low (all lanes signal detected in 2-lane operation)
- LOS[3:0] goes low (all lanes signal detected in 4-lane operation)
- ANYLOS goes low (all lanes signal detected in 8-lane operation)

Note: Some links startup cleanly (within 300 nS of de-assertion of LOS flag), but others do not. The probe itself can not achieve lock quickly until it receives a stable signal and a stable reference clock. Signal detection does not imply a valid serial data signal. Signal detection (LOS status) is delayed relative to link data capture.

10b Mode Debug

The FS4400 requires an external reference clock connection when used in 10b mode.

The LEDs operate as described previously.

Note: When using the FS4400 in 10-bit Mode, the user must select a Logic Analyzer Configuration file based on the lane width of the link being probed. The user must also select the correct lane width in the Probe Config window.

The probe hardware does real-time, lane-based 8b10b error checking, lane deskew and lane deskew checking. There are no filters or pattern recognizers provided in 10b mode. Packets and ordered sets are detectable using the analyzer trigger capabilities, looking for the values listed below. There is no inverse assembler; however there are pre-defined symbols that make packet boundaries visible in the state listing.

The following are some useful 10b symbol definitions for PCI-Express. All but the TSID values are available pre-loaded in the lane data symbol tables for convenient setup of triggers. Trigger on COM to find any ordered set. Trigger on FTS, SKP or IDL to find specific ordered sets. Trigger on SDP to find DLLP packets. Trigger on STP to find TLP packets. Remember there are usually two different possible codes representing each character in 10-bit Mode.

COM	K28.5
FTS	K28.1
SKP	K28.0
SDP	K28.2
IDL	K28.3
PAD	K23.7
STP	K27.7
END	K29.7
EDB	K30.7
TSID1	D10.2
TSID2	D5.2

Value follows negative disparity		
COM+	0101_111100	17C
FTS+	1001_111100	27C
SKP+	0010_111100	0BC
SDP+	1010_111100	2BC
IDL+	1100_111100	33C
PAD+	0001_010111	057
STP+	0001_011011	05B
END+	0001_011101	05D
EDB+	0001_011110	05E
TSID1	1010_101010	2AA
TSID2	1010_100101	2A5

Value follows positive disparity		
COM-	1010_000011	283
FTS-	0110_000011	183
SKP-	1101_000011	343
SDP-	0101_000011	143
IDL-	0011_000011	0C3
PAD-	1110_101000	3A8
STP-	1110_100100	3A4
END-	1110_100010	3A2
EDB-	1110_100001	3A1
TSID1	1010_101010	2AA
TSID2	1010_100101	2A5

Verify Setup in 10-bit Mode:

To verify correct lane reverse settings, make sure the SDP, STP characters appear on the leftmost lane and the END characters appear on the rightmost lane.

To verify lane width settings, verify Data LED is green (checks for valid data on all lanes, and the successful de-skew of active lanes). Observe a DLLP packet in the listing and verify it consists of 8 consecutive bytes from SDP through END.

To verify correct lane inversion settings, check that the TSID (last 10 states of every TS1 or TS2 ordered set) during training is hex 2AA or 2A5 and not 155 or 15A.

Finding Stable PCIe Link Activity in 10-bit Mode:

When a link is expected to perform initialization, set the analyzer to trigger on:

- "Lane0 = TSID2 (2A5), 10 times Consecutively"

This detects TS2 ordered sets during link initialization. This assures the link is up and running because a PCIe device issues TS2 ordered sets only after it has received valid TS1 ordered sets from the other direction.

Finding Link Startup During Fast Training in 10-bit Mode:

When a link is expected to perform fast training, set the analyzer to trigger on:

- "Lane0 = FTS+ or FTS-"

Finding the start of Signal Activity in 10-bit Mode:

Set the analyzer to trigger on signal detection status (LOS = loss of signal). Note this method can only be used when the probe is not setup for ASPM mode:

- ANYLOS goes low (all lanes signal detected)

Note: Some links startup cleanly (within 300 nS of de-assertion of LOS flag), but others do not. The probe itself can not achieve lock quickly until it receives a stable signal and a stable reference clock. Signal detection does not imply a valid serial data signal. Signal detection (LOS status) is delayed relative to link data capture.

Finding the first Idle Characters in 10-bit Mode:

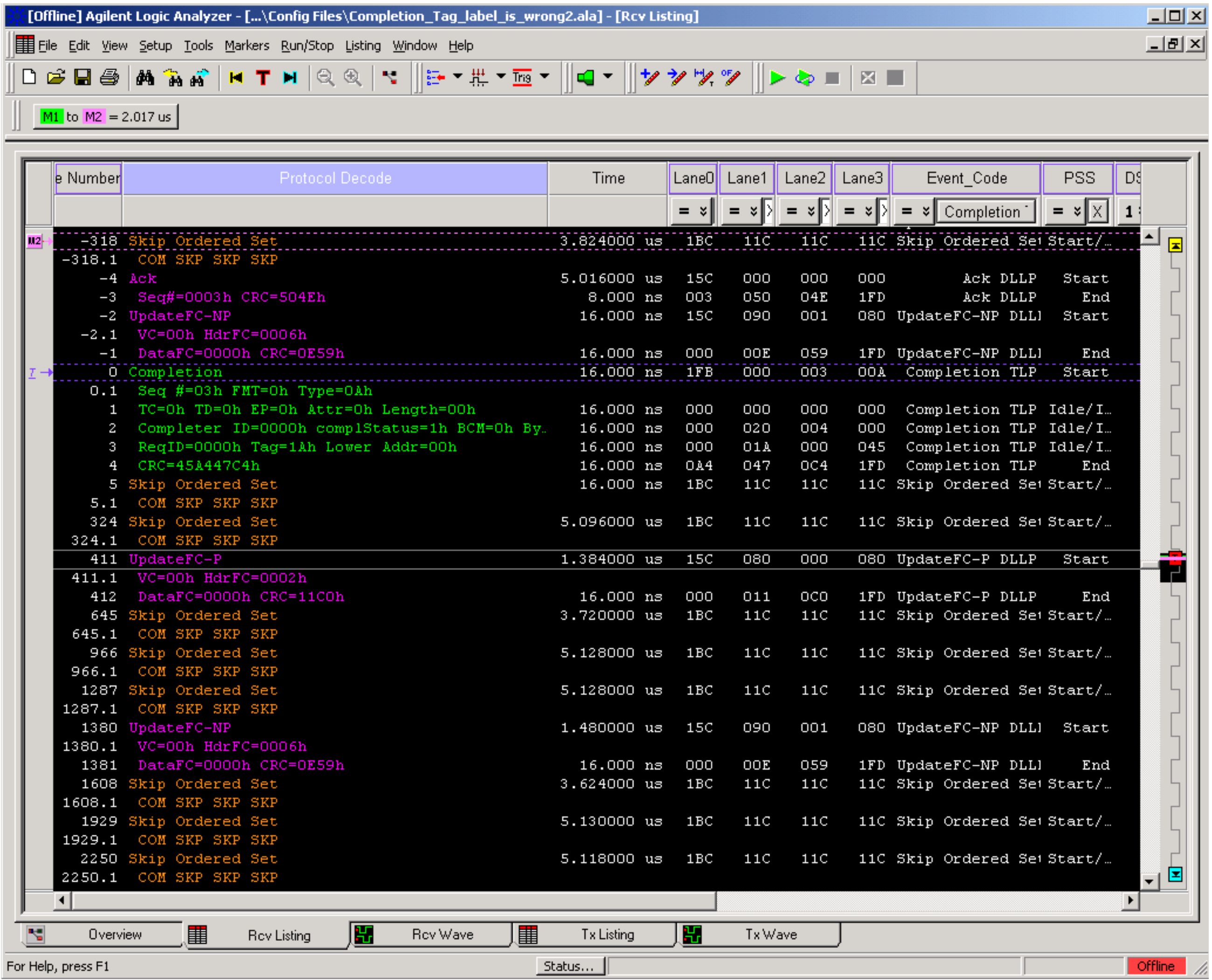
With scrambling assumed to be occurring, the first 2 idle data words following TS1/TS2 training sets will be either, (depending on disparity):

- 2CD followed by 161
- 10D followed by 15E

Note: Idle data might not immediately follow TS1/TS2, there may be Skip Ordered Sets or DLLPs

The State Listing Display

Captured data is as shown in the following figure. The below figure displays the protocol decode.



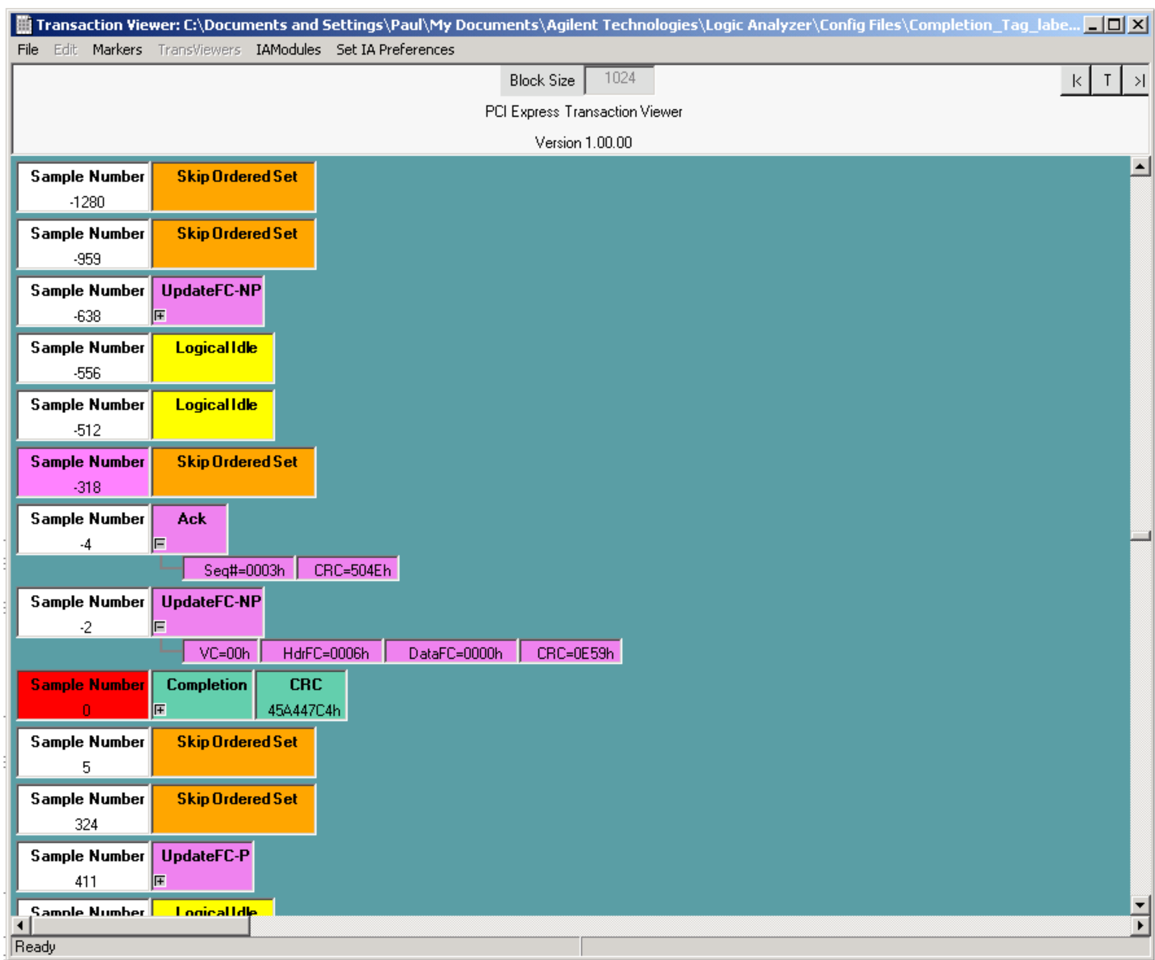
The FS4400 Decode Software will perform the following functions:

- Decode all PCI Express command and cycle types
- Color code the transaction type. The colors used by the software are as follows:
  - Ordered Sets: Orange
  - TLP Packets: Green.
  - DLLP: Purple
  - Error: Red
  - Signal (Probe generated packets): Yellow
  - Unknowns: White

Transaction Viewer

The FS4400 Protocol Decoder is fully integrated with the FuturePlus Systems Transaction Viewer application.

This following figure is an example Transaction Viewer.



The Transaction Viewer is a powerful tool that allows the user to view data captured with the FS4400 in a graphical environment that presents the information by Transaction as opposed to State.

This tool is integrated with State Listing on the 16900 and allows marker and trigger settings to be shared between the Protocol Decoder and the Transaction Viewer.

The Transaction Viewer itself is a separate application that needs to be downloaded from the FuturePlus Systems website: www.futureplus.com. The user manual for the Transaction Viewer is also separate and can be found either on the FuturePlus Systems Documentation CD on the FuturePlus Systems website.

The screen listed above displays the same set of transactions that are contained in the previous sections' IA trace protocol decode screen

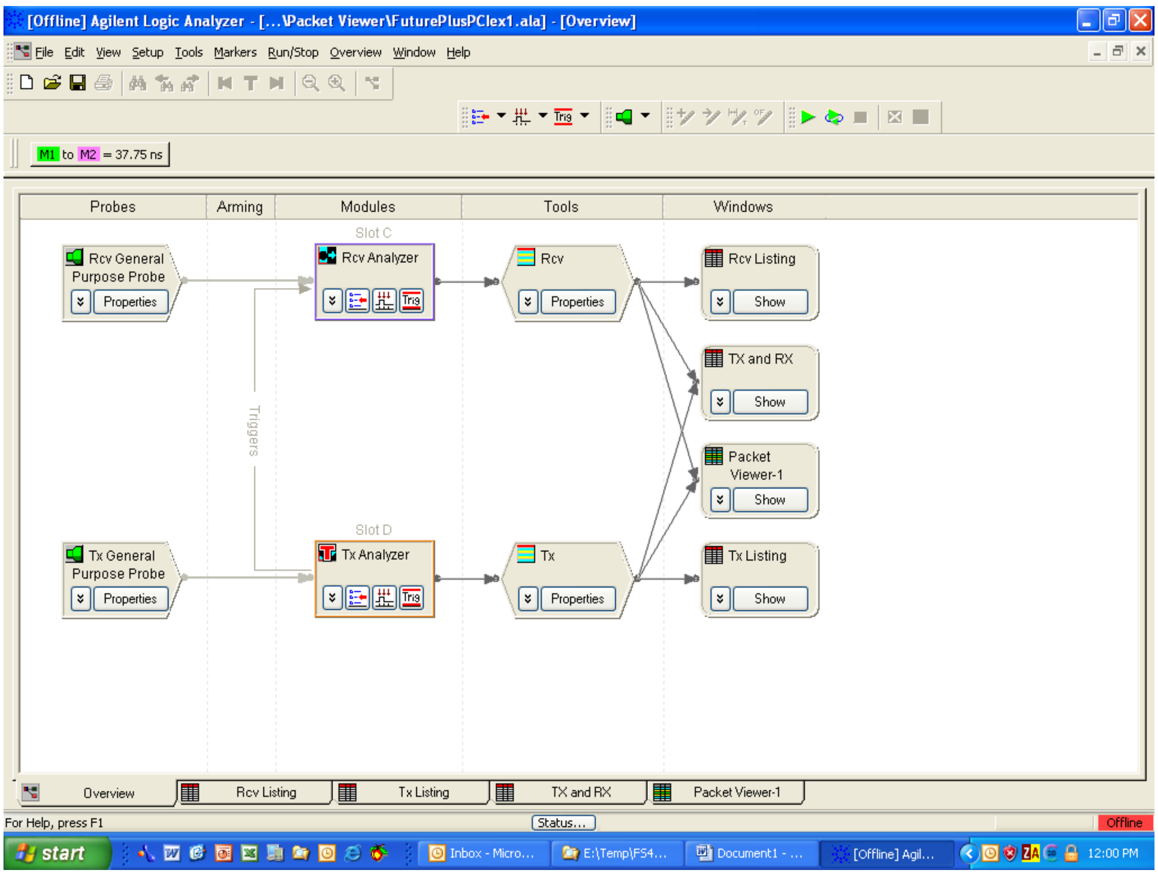
As you can see, the level of detail has been brought up to the transactional level with the effect of allowing the new tool to show a much greater range of decoded trace states.

Packet Viewer Tool

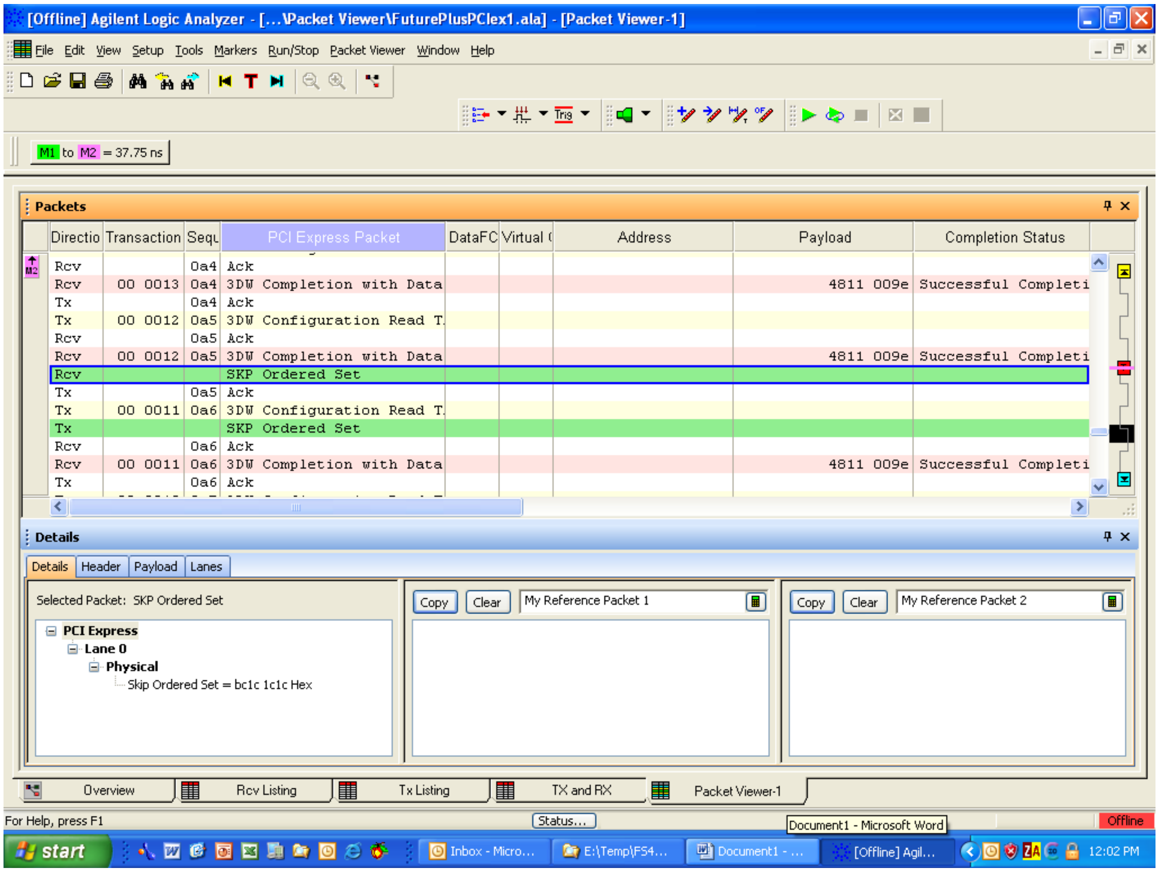
The Packet Viewer tool is provided as part of v3.50 of the Agilent Logic analyzer software. The configuration files provided with the FS4400 include the xml files that allow the use of the Packet Viewer functionality within the 1690x and 1680x environments.

To set-up the Packet Viewer start from the logic analyzer Overview screen and select “New Packet Decoder” from the Tools drop down menu. You will be asked where to insert this tool, we recommend After the PCIe Analyzer and before the PCIe Inverse assembler. Next, select PCI Express as the Protocol Family and then select the appropriate link width for the application. Do this for both directions of the link that is being probed.

Next, select “New Packet Viewer” from the Window drop-down menu and place it after the 2 Packet Decoders. The logic analyzer overview should look as show below:



The Packet Viewer information is displayed as a separate tab in the logic analyzer application. The overall function of this tool is to display information at the packet level while providing windows that provide some more packet data detail or reference information.



There is more detailed information on the Packet Decoder and Packet Viewer in the Agilent logic analyzer Help files contained in v3.50 or higher.

General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS4400 probe.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4400 probe.

If the product is used in a manner not specified by manufacturer, then the protection provided by the equipment may become impaired.

Standards Supported

PCI Express Base Specification, Revision 1.0a and 1.1

Power Requirements

100-240VAC, 2 amps.

Logic Analyzer Required

Agilent 16715/6/7/9 or 16750/1/2 installed in the 16700A or 16700B frame, 16753 cards or better are recommended. 16910/11 or 16950 cards can be used in the 16900 frame. 1680x analyzers. See section on Connecting to the analyzer.

Number of Probes Used

The State Adapter Probe interface uses 8 cable headers of either the 40 pin or 80 pin type.

Logic Analyzer State Clock Frequency

125MHz for x1 PCI Express Protocol Analysis or 250MHz for x2, x4 or x8. 250 MHz for x1 x2 x4 or x8 PCI Express 10b analysis.

Environmental Temperature

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Operating: 20 to 30 degrees C (68 – 86 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 80% relative humidity. Avoid sudden, extreme temperature changes which would cause condensation on the FS4400 module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the FS4400 module. If a failure is suspected in the FS4400 module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the FS4400 is module replacement. However, if parts of the FS4400 module are damaged or lost contact the factory for a list of replacement parts.

Signal Connections

The FS4400 contains 8 90 pin Samtec pod connections and a duplicate 8 40 pin pod connections for use with older logic analyzer modules. These are wired in parallel and both sets of connections are always driven by the FS4400

The following is the pinout configuration of the connectors, (repeat for 2nd link-direction – "B" pods)

LAI Bit Definitions for a Single Direction x1, x2, x4 Link PCIe mode

(4 Pods, 1 machine)

Field	Bits	Definition	Pod	Bits
Default Store Flag	1	1= Store this state 0 = Discard	A4 (B4)	16
8b/10b Mode	1	0= Data is 8 bit decoded 1 = Data is 10 bit encoded		15
Aligned	1	1= Multi-lane link is word-aligned (bonded)		14
Data Error	1	1= This state includes an error		13
In reset	1	1= This state affected by SYSRST		12
Packet Recognizer	3	1= Packet recognized (pulsed for one clock cycle during packet)		11:9
Spare	3	presently unused		8:6
Packet Sample State	2	10=start, 01=end, 11=start & end 00=inside packet, ordered set or Idle		5:4
Event Code	6	Describes what type of packet, ordered set, signal event or error event. Code is held for duration of packet or ordered set, except that signal and error events can over-write any state except the start state. When start and end coincide, the event code for the starting packet is displayed.	 A3 (B3)	3:0 16:15
Data Present [3,2,1,0]	4	1= Corresponding lane data byte is present. 0= Data not present. "Not present" is due to lane spreading of x1 and x2 to 4 lane format.		14:11
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect Logically named, reflects lane reverse status.		10:7
Lane 0 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation. 10b Mode: Becomes 10b encoded data bit 9		6
Lane 0 Control Flag	1	1=K character (control) 0= D character (data) 10b Mode: Becomes 10b encoded data bit 8		5
Lane 0 8b Data	8	Decoded 8b value 10b Mode: Becomes 10b encoded data bits 0-7	 A2 (B2)	4:0 16:14
Lane 1 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation. 10b Mode: Becomes 10b encoded data bit 9		13
Lane 1 Control Flag	1	1=K character (control) 0= D character (data) 10b Mode: Becomes 10b encoded data bit 8		12
Lane 1 8b Data	8	Decoded 8b value 10b Mode: Becomes 10b encoded data bits 0-7		11:4
Lane 2 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation. 10b Mode: Becomes 10b encoded data bit 9		3
Lane 2 Control Flag	1	1=K character (control) 0= D character (data) 10b Mode: Becomes 10b encoded data bit 8		2
Lane 2 8b Data	8	Decoded 8b value 10b Mode: Becomes 10b encoded data bits 0-7	 A1 (B1)	1:0 15:10
Lane 3 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation. 10b Mode: Becomes 10b encoded data bit 9		9
Lane 3 Control Flag	1	1=K character (control) 0= D character (data) 10b Mode: Becomes 10b encoded data bit 8		8
Lane 3 8b Data	8	Decoded 8b value 10b Mode: Becomes 10b encoded data bits 0-7		7:0

The clock is on A1 bit 16 (B1 bit 16).

LAI Bit Definitions For a Single Direction x8 Link PCIe mode

Field	Bits	Definition	Pod	Bits
		(Pod A4 is unused)	A4	
		(Pod A3 is unused)	A3	
Lane 0 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.	A2	16
Lane 0 Control Flag	1	1=K character (control) 0= D character (data)		15
Lane 0 8b Data	8	Decoded 8b value		14:7
Lane 1 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		6
Lane 1 Control Flag	1	1=K character (control) 0= D character (data)		5
Lane 1 8b Data	8	Decoded 8b value		4:0
			A1	16:14
Lane 2 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		13
Lane 2 Control Flag	1	1=K character (control) 0= D character (data)		12
Lane 2 8b Data	8	Decoded 8b value		11:4
Lane 3 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		3
Lane 3 Control Flag	1	1=K character (control) 0= D character (data)		2
Lane 3 8b Data	8	Decoded 8b value		1:0
			B4	16:11
Default Store Flag	1	1= Store this state 0 = Discard		10
Aligned	1	1= Multi-lane link is word-aligned (bonded)		9
Data Error	1	1= This state includes an error		8
Packet Recognizer	3	1= Packet recognized (pulsed for one clock cycle during packet)		7:5
Unjust	1	1=TLP or DLLP Packet starts in Lane 4		4
Packet Sample State	2	PSS[1] = SOP (start of packet or ordered set) PSS[0] = EOP (end of packet or ordered set) 10=start, 01=end, 11=start & end 00=inside packet, inside ordered set or Idle		3:2
Event Code	6	Describes what type of packet, ordered set, signal event or error event. Code is held for duration of packet or ordered set, except that signal and error events can over-write any state except the start state. When start and end coincide, the event code for the starting packet is displayed.		1:0
			B3	16:13
Any LOS	1	1= Any active lane has Loss of Signal 0= All active lanes have Signal detect		12
Lane 4 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		11
Lane 4 Control Flag	1	1=K character (control) 0= D character (data)		10
Lane 4 8b Data	8	Decoded 8b value		9:2
Lane 5 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		1
Lane 5 Control Flag	1	1=K character (control) 0= D character (data)		0
Lane 5 8b Data	8	Decoded 8b value	B2	16:9
Lane 6 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		8
Lane 6 Control Flag	1	1=K character (control) 0= D character (data)		7
Lane 6 8b Data	8	Decoded 8b value		6:0
			B1	15
Lane 7 Sym Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		14
Lane 7 Control Flag	1	1=K character (control) 0= D character (data)		13
Lane 7 8b Data	8	Decoded 8b value		12:5
Spare	5	Unused bits		4:0

LAI Bit Definitions for a Single Direction x2, x4 Link 10b mode

(4 Pods, 1 machine)

Field	Bits	Definition	Pod	Bits
Unused	12	Set to 0	A4 B4	16:5
Align Flag	1	1 = Alignment of multi-lane link detected		4
Any Invalid Error Flag	1	1 = This state includes a 10B code error (disparity or decode) in any active lane.		3
LOS[3,2,1,0]	4	1 = Corresponding lane Loss of Signal. 0 = Signal detect.		2:0
			A3 B3	16
ANY LOS	1	1 = Any Lane Loss of Signal 0= Signal detect on all active lanes		15
Lane 0 Disparity Error	1	1 = Lane data is the wrong 10B disparity		14
Lane 0 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		13
Lane 0 10B Data	10	Encoded 10b value		12:3
Lane 1 Disparity Error	1	1 = Lane data is the wrong 10B disparity		2
Lane 1Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		1
Lane 1 10B Data	10	Encoded 10b value		0
			A2 B2	16:8
Lane 2 Disparity Error	1	1 = Lane data is the wrong 10B disparity		7
Lane 2 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		6
Lane 2 10B Data	10	Encoded 10b value		5:0
			A1 B1	15:12
Lane 3 Disparity Error	1	1 = Lane data is the wrong 10B disparity		11
Lane 3 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		10
Lane 3 10B Data	10	Encoded 10b value		9:0

The clock is on A1 bit 16 (B1 bit 16).

LAI Bit Definitions For a Single Direction X1 Link

(1 Pod, 1 machine) (repeat for 2nd link-direction)

Field	Bits	Definition	Pod	Bits
ANY LOS	1	1 = Any Lane Loss of Signal 0= Signal detect on all active lanes	A1 B1	15
Lane 0 Disparity Error	1	1 = Lane data is the wrong 10B disparity		14
Lane 0 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		13
Lane0	10	Encoded 10b value		12:3
Unused	2	Set to 0		2:1
Any Invalid Error Flag	1	1 = This state includes a 10B code error (disparity or decode) in any active lane.		0

The clock is on A1 bit 16 (B1 bit 16).

LAI Bit Definitions For a Single Direction x8 Link 10b mode

(6 Pods, 1 machine)

Field	Bits	Definition	Pod	Bits
Unused	1	Set = 0	A2	16
Align Flag	1	1 = Alignment of multi-lane link detected		15
Any Invalid Error Flag	1	1 = This state includes a 10B code error (disparity or decode) in any active lane.		14
Any LOS	1	1 = Any Lane Loss of Signal 0= Signal detect		13
Lane 0 Disparity Error	1	1 = Lane data is the wrong 10B disparity		12
Lane 0 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		11
Lane 0 10B Data	10	Encoded 10b value		10:1
Lane 1 Disparity Error	1	1 = Lane data is the wrong 10B disparity		0
Lane 1 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode	A1	15
Lane 1 10B Data	10	Encoded 10b value		14:5
Lane 2 Disparity Error	1	1 = Lane data is the wrong 10B disparity		4
Lane 2 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		3
Lane 2 10B Data	10	Encoded 10b value		2:0
			B4	16:10
Lane 3 Disparity Error	1	1 = Lane data is the wrong 10B disparity		9
Lane 3 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		8
Lane 3 10B Data	10	Encoded 10b value		7:0
			B3	16:15
Lane 4 Disparity Error	1	1 = Lane data is the wrong 10B disparity		14
Lane 4 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		13
Lane 4 10B Data	10	Encoded 10b value		12:3
Lane 5 Disparity Error	1	1 = Lane data is the wrong 10B disparity		2
Lane 5Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		1
Lane 5 10B Data	10	Encoded 10b value		0
			B2	16:8
Lane 6 Disparity Error	1	1 = Lane data is the wrong 10B disparity		7
Lane 6 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		6
Lane 6 10B Data	10	Encoded 10b value		5:0
			B1	15:12
Lane 7 Disparity Error	1	1 = Lane data is the wrong 10B disparity		11
Lane 7 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		10
Lane 7 10B Data	10	Encoded 10b value		9:0

The clock is on B1 bit 16.